TUNELLING LEAKAGE CURRENT CHARACTERIZATION OF SILICON OXIDE AND HIGH-k DIELECTICS FOR ADVANCED SEMICONDUCTOR DEVICES

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Abstract–*The continuum down-scaling lead the field-effect transistors in the nanometre region with devices and structures characterized by high doping drains/ sources and thin insulating layers. When the thickness of the layers attends 2nm or less, the coupling between the semiconductor channel and the gate can't be neglected. A correct quantum-mechanical model must correct evaluate the channel charge distribution and the leakage current flowing between the gate and the channel through tunnelling. The presented iterative approximation method for calculate the 1D device main electric parameters offer short time computation and was applied to study the thin silicon oxide and high-k dielectrics stacks combination for the silicon devices.*

Keywords: *CMOS, high-k dielectrics gate, leakage currents, tunnelling, quantum-mechanical model.*

1. INTRODUCTION

High-k dielectric oxides are presently investigated as alternative gate dielectric films for complementary metal oxide silicon-CMOS transistors. The continuous decrease of ultra-large-scale integration dimensions determines that SiO_2 gate dielectric attends critical dimensions of tens of Å and reaches fundamental limitations in preventing current leakage from the gate into the channel. One possible solution is to replace SiO_2 with higher permittivity insulator materials. Among the promising candidate materials investigated are HfO_2, $HfSiO_4$, $ZrSiO_4$, La_2O_3 and Y_2O_3. There are however presently important issues related to the integration of these materials and that makes highly desirable to previously understand how the new materials properties affects the functionality of CMOS devices. A correct quantum-mechanical model must properly evaluate the channel charge distribution and the leakage current flowing between the gate and the channel through tunnelling. Consequently the gate, the insulator and the substrate semiconductor channel must be considered like a single space region accessible to all free charge carriers. Looking from the gate this high quality thin oxide is responsible for the continued increase of the gate leakage, which increase the power consumption of integrated circuits [1]. The understanding of the MOS system in z direction begins very important for research the tunnelling current in EEPROM devices and also in high performance MOS devices with ultra thin oxides [2].

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2. THE GATE LEAKAGE CURRENTS

The charge distribution and quantum-mechanical leakage currents in ultra thin metal-insulator-semiconductor gate stacks composed of several layers materials are very important [3]. Considering all the capacitor like a single quantum mechanical quantity the effective mass approximation for the electrons in the different valley and the Hartree approximation for the electron-electron interaction in inversion layer, the Schrödinger-Poisson equation can be solved. Because the insulating layer is relatively thin but the energy barriers separating the inversion layer from the gate electrode is high enough to prevent the flow of electrons to the gate, the potential well host the majority of inversion layer electrons and the channel is coupled only weakly with the gate [4].

3. THE ITERATIVE APPROXIMATION METHOD

The first fully numerical self-consistent results of the inverted MOS structure were mainly attributed to Stern [5]. Then the self–consistent solution has been extended to holes in inverted pMOS structure [6]. The quantum mechanical treatment of the MOS structure in the accumulation regime was described by Sune [7]. The self-consistent Schrödinger-Poisson equations were applicable to an inverted structure in the next approximations: the effective mass approximation, the ideal interface semiconductor-oxide and interruption of wave function at interface semiconductor-oxide. The time-independent Schrödinger equation in 3D space, using the position vector $\mathbf{R}=(\mathbf{r},z)$ can be formally written:

$$H\psi(\mathbf{r}, z) = E\psi(\mathbf{r}, z), \qquad (2.1)$$

where $\psi(\mathbf{r},z)$ is the wave function, E is the

eigenvalue energy, H is the system Hamiltonian, composed from kinetic energy T and potential energy W. For long channel device the potential profile is mainly one dimensional and the drain and source regions can be considered like electrons reservoirs for the inversion layer. The 1D simplification allows using the wave operator like a function of the z coordinate only:

$$\psi(\mathbf{r},z) = \phi(z)e^{i\mathbf{k}\cdot\mathbf{r}}, \quad (2.2)$$

where $\mathbf{k}=(k_x,k_y)$ is the wave vector in the (x,y) plane. So the carrier are quantized in the z direction and are free to move in the $\mathbf{r}=(x,y)$ plane, with a continuous energy component. After a phase transformation and imposing the constraint of vanishing for the first derivative of the wave function, the envelope 1D time-independent reduced equation (2.1) is:

$$-\frac{\hbar^2}{2m_{zz}}\psi''(z) + W\psi = E_z\psi(z), \quad (2.3)$$

where $\hbar$ is reduced Planck constant, m_{zz} is the effective masses in m_o units, W is potential energy, $\Psi(z)$ is the 1D envelope wave functions and E_z is the eingenvalue energy.

Considering the MOS structure a quantum mechanical system, an externally applied gate bias induces a potential well that confines carriers in the region of the semiconductor-oxide interface. The electrostatic potential and charge respect the Poisson equation in any z direction from silicon region:

$$\frac{d^2V(z)}{dz^2} = -\frac{1}{k_{Si}\varepsilon_0}\rho(z), \quad (2.4)$$

where $V(z)$ is the electrostatic potential, $\rho(z)$ is the charge density, k_{Si} is the Si relative dielectric constant. Assuming the p-type substrate with completely ionized impurities and neglecting the hole concentration in inversion can approximate the charge density:

$$\rho(z) = \rho_{depl}(z) - qn(z), \quad (2.5)$$

where ρ_{depl} is the depletion layer charge and $n(z)$ is the carrier's distribution.

Close to the interface the electrons have a position dependent concentration proportional with the probability density and a sum of each energy valley and subband.

$$n(z) = \sum_{i,j} n_{i,j}(z) = \sum_{i,j} N_{ij}^{(2D)}(E_{z,ij}, E_F)\left|\psi(z)\right|^2, \quad (2.6)$$

where $N_{ij}^{(2D)}$ is the subband population which integrates the all possible energies of a subband of the 2D density of states, $\left|\psi(z)\right|^2$ is the probability density, $E_{z,ij}$ is the solution of 1D Schrödinger equation (2.3) and represents the discrete bottom level of a particular energy subband j, for each valley i and E_F is Fermi energy level. The carrier's distribution can be more detailed using the valley and spin degeneracy and Fermi-Dirac statistics. The assumption that the silicon-oxide interface is ideally, was technologically realized by election the [001] surface orientation which minimizes the dangling bonds at the interface, resulting a high quality interface after passivation.

Considering the quantization effects of silicon-insulator interface an approximate geometrical solution to calculate the charge densities and subband energy levels reduces consistently the computational complexity for leakage current evaluation. Using the same effective mass approximation the areal density of charge in the inversion layer is:

$$N_{inv} = \sum_{i,j}\oint_z N_{ij}^{(2D)}(E_{z,ij}, E_F)\left|\psi(z)\right|^2 dz = \sum_{i,j} N_{ij}^{(2D)}(E_{z,ij}, E_F) \quad (2.7)$$

Using the geometrical approximation of Si band bending in inversion [8] the energy level is:

$$E_{z,ij} = \left(\frac{\hbar^2}{2m_{z,i}}\right)^{1/3}\left(\pi q F_{ef}\frac{3}{2}\left(j+\frac{3}{4}\right)\right)^{2/3} \quad (2.8)$$

and the subband charge is:

$$q_{ij} = \frac{2E_{z,ij}}{3qF_{ef}}, \quad (2.9)$$

where F_{ef} is the $E_{z,ij}$ corresponding effective electric field. Then the inversion charge is:

$$q_{inv} = \sum_{i,j} q_{i,j}\frac{N_{i,j}^{(2D)}}{N_{inv}}, \quad (2.10)$$

and the total silicon surface bending:

$$\Psi_S = \Psi_D + q\frac{N_{inv}q_{inv}}{k_{Si}\varepsilon_0} + \frac{k_BT}{q} \quad (2.11)$$

where Ψ_S is the surface potential, Ψ_D is the drop voltage at surface due to space charge region. The last term is the influence of doping concentration to charge region [8]. Using the charge boundary conditions the equations can be iteratively solved to attain the convergence in the next sequence:

1. Guess the initial N_{inv}, Ψ_S and Ψ_D
2. Consider charge boundary condition $N_{inv\text{-}bc}$
3. Iterate Ψ_S with condition $N_{inv}(\Psi_S)/N_{inv\text{-}bc}\rightarrow 1$
4. Iterate Ψ_D with condition $\Delta\Psi_D\rightarrow 0$
5. Compute the potential distribution

We have possible loops from out to input, of step 3 and 4 and from out of step 4 to input of step 3. The method can be used also for tunnelling based leakage currents in high-k dielectric stach.

4. RESULTS

For numerical simulations we used the ATLAS devices simulator software package from Silvaco. The main module program used is presented in Fig. 1, in order to generate the MOS structure presented in fig. 2. Then was calculated the gate current, Fig. 3 and the capacity from gate to substrate, Fig. 4, function of polysilicon doping concentrations 10^{19}cm^{-3}, 10^{20}cm^{-3} and 10^{21}cm^{-3}.

```
mesh
x.mesh loc=-0.01 spac=0.01
x.mesh loc=0.01  spac=0.01
y.mesh loc=-0.04 spac=0.001
y.mesh loc=0.02  spac=0.001
region number=1 x.min=-0.01 x.max=0.01 y.min=-0.04 y.max=-0.03  \
       material=aluminum
region number=2 x.min=-0.01 x.max=0.01 y.min=-0.03 y.max=-0.005 \
       material=poly
region number=3 x.min=-0.01 x.max=0.01 y.min=-0.005 y.max=0.0   \
       material=oxide
region number=4 x.min=-0.01 x.max=0.01 y.min=0.0 y.max=0.02     \
       material=silicon
electrode x.min=-0.01 x.max=0.01 y.min=-0.04 y.max=-0.03 name=gate
electrode bottom name=substrate
doping region=2 p.type concentration=1e19 uniform
doping region=4 p.type concentration=1e17 uniform
solve init
solve vgate=-1.5
solve vgate=-3
save outfile=mos2ex15-3V19.str
# tonyplot mos2ex15-3V19.str -set mos2ex15_BD.set
log outfile=mos2ex15_CV19.log
solve vgate=-2.8 vstep=0.2 vfinal=3.0 name=gate ac freq=1e6
previous
tonyplot mos2ex15_CV19.log -set mos2ex15_CV.set
```

Fig. 1. The main ATLAS program module.

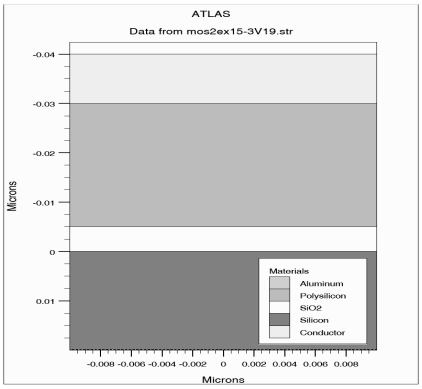

Fig. 2. The device structure.

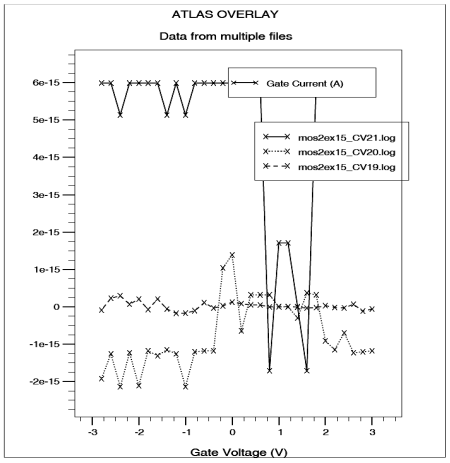

Fig. 3. The Gate Current.

The first numerical simulations proves the dependence of leakage current, Fig. 3 and depletion effect Fig. 4, function of doping concentration like considered in chapter 3. Using the barrier height of 3.1eV, substrate doping $5\times10^{17}cm^{-3}$, effective silicon oxide mass of $0.5m_o$ and donor poly doping 6×10^{19} the results of short computation iterative approximation of silicon oxide current gate density, Fig. 5, was in good agreement with experimental gate current density curves presented in [9].

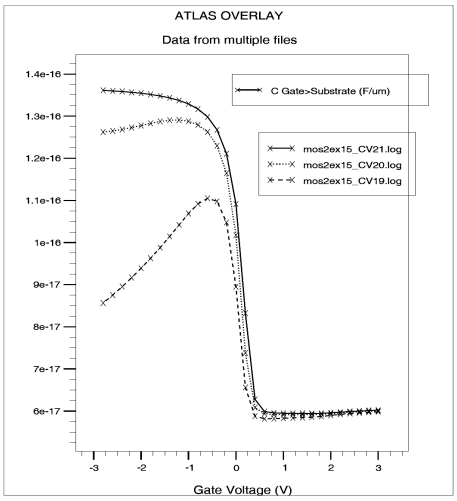

Fig. 4. The Gate-Substrate Capacity.

A little overestimation of leakage current at high gate bias voltage is observed also in other reports, [9] and [10], based of approximation of Fermi level by the value in the bulk silicon substrate.

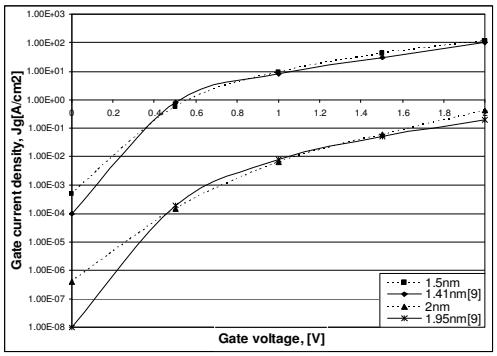

Fig. 5. Silicon oxide gate current density calculated (1.5nm and 2nm) and experimental curves presented in [9], (1.41nm[9] and 1.95nm[9]).

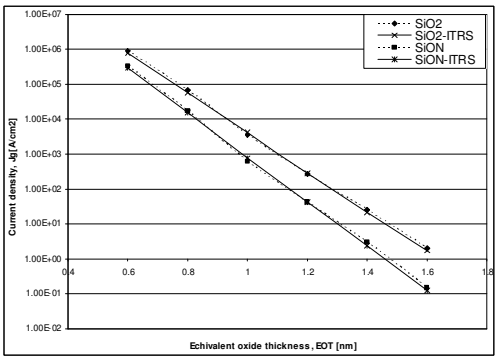

Fig. 6. Simulated and ITRS tunnelling current gate leakage in inversion channel for oxide and oxynitride at Vg=1V.

The polysilicon doping level suppresses the gate leakage current for gate bias in inversion because the additional voltage drops over the depleted layer, [11]. This solution decreases the drive capacitance and the device performances. The substrate doping level

affects the leakage current through the surface potential of the channel. Because increasing the physical thickness of gate dielectric affects the device parameters like drive current, a compromise solution is to increase the dielectric constant using the SiON layer with dielectric constant up to 7.6 for Si_3N_4. The performances of SiON like gate dielectric are better than SiO_2 as in Fig. 6, according with simulations and ITRS. Comparing the calculated data with gate leakage current through Al_2O_3 high-k dielectric stacks presented in [12] a good fit was obtained, Fig. 7.

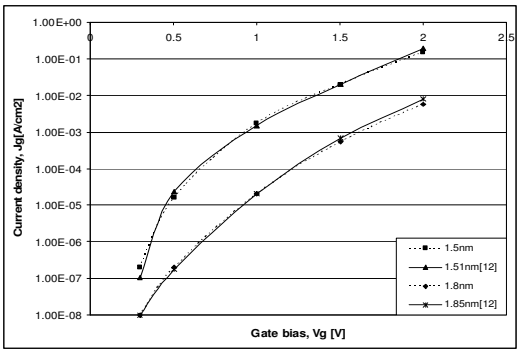

Fig. 7. Calculated data and experimental gate leakage currents [12], for Al_2O_3 high-k stacks.

5. CONCLUSIONS

High-k atomic layer deposition stacks like insulating in the metal-insulating-semiconductor structure was studied. An iterative approximate method to calculate the 1D MOS structures main electric parameters without using the Schrödinger-Poisson equations is used. This method is based on approximation of effective field function of doping parameters. The tunnelling currents can be calculated more rapidly and the study for different gate dielectric stacks can be made. The precision can be increased by 2D or 3D analysis of Schrödinger-Poisson equations. The main application is to calculate the direct tunnelling current due to the thin oxide layers. The method is extensible to high-k dielectric stacks in order to study the influence of several material parameters like the impact of layer thickness on gate leakage and the approach of gate stack scalability. The results obtained using numerical calculation show that the increase of the gate dielectric constant has a very important effect in reducing the leakage currents. Comparing the results from Fig. 5 and 7 for 1V gate bias and 1.5nm thickness the increase of dielectric constant to 7 reduce the leakage current with 4 order of magnitude. Other simulations show that the leakage current decrease significant when the interfacing oxide is completely eliminated. Future works will be focus of other high-k dielectric stacks like HfO_2, $HfSiO_4$, $ZrSiO_4$, La_2O_3, and Y_2O_3.

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