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Improved Linearity CMOS Multifunctional Structure for VLSI Applications

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Abstract. An original improved linearity multifunctional structure designed for VLSI applications will be further presented. The core of the circuit is represented by a differential amplifier based on an original linearization technique. The great advantages of the increased modularity and controllability and of the reduced design costs associated represent an immediate consequence of the multiple functions realized by the proposed structure: amplifying, multiplying or simulating positive and negative resistances. The frequency response and the linearity are strongly increased by implementing original techniques, while the silicon occupied area per function is reduced as a result of the multifunctionality. The simulation confirms the estimated results, showing a linearity error less than a percent for a small value of the supply voltage ±3 V and for an extended input range ±500 mV.

1. Introduction

A very important trend in VLSI designs, especially for submicronic technologies is the continuous reducing of the layout area. In CMOS circuits, parasitic bipolar transistors and especially classical resistors having a surface consumption proportional to the value of the resistance represent the largest area consumers. Thus, is not efficient to obtain resistances greater than 10 kΩ using the classical approach. The new method for reducing the occupied area for large values of the equivalent resistance is to implement a circuit named *active resistor* using exclusively MOS transistors for simulating a linear current-voltage characteristic.

An important class of these circuits, referring to the active resistors with controllable negative equivalent resistance, covers a specific area of VLSI designs, finding

very large domains of applications such as the canceling of an operational amplifier load or the design of integrators with improved performances.

The first generation of MOS active resistors [1], [2] used MOS transistors working in the linear region, having the main disadvantages of an equivalent resistance inherently nonlinear and of obtaining distortion components that are complex functions on MOS technological parameters. A better design of CMOS active resistors is based on MOS transistors working in saturation [3], [4], [5]. Because of the quadratic characteristic of the MOS transistor, some linearisation techniques were developed in order to minimize the nonlinear terms from the current-voltage law of the active resistor. Usually, the linearisation of the $I - V$ characteristic is obtained in a first-order analysis. However, the second-order effects which affect the MOS transistor operation (mobility degradation, bulk effect and channel length modulation) limits the circuit linearity introducing odd and even-order distortions, as shown in [4].

An important goal in VLSI designs is represented by the possibility of a multiple use for the same cell, the increased modularity that could be achieved being reflected in an important reductions of the design costs.

The original idea is to use a particular implementation of a CMOS differential amplifier based on the constant sum of the gate-source voltage for obtaining (with minor changes in the design) three important functions:

- The signal gain with theoretical null distortions;
- Simulation (in a first-order analysis) of a perfect linear resistor using exclusively MOS active devices, having the advantages of a very good controlability of the equivalent resistance and of an important reduction of the silicon occupied area, especially for large value of the simulated resistance;
- Simulation of a controllable negative resistance circuit with improved linearity.

2. Theoretical analysis

2.1. The linear differential amplifier

2.1.1. The implementation of the linear differential amplifier

The proposed implementation of the differential amplifier representing the core of the multifunctional structure uses exclusively MOS transistors biased in saturation region for improving the frequency response and exploits the original principle of the constant sum of gate-source voltages for obtaining a theoretical zero value of the total harmonic distortions. The multiple impact of this last advantage is referring to the removing of the superior-order harmonics from the output voltage of the differential amplifier and to a very accurate simulation of the linear current-voltage characteristic of both positive and negative equivalent-resistance circuits. The implementation in CMOS technology of the previous mentioned differential amplifier is presented in Fig. 1.

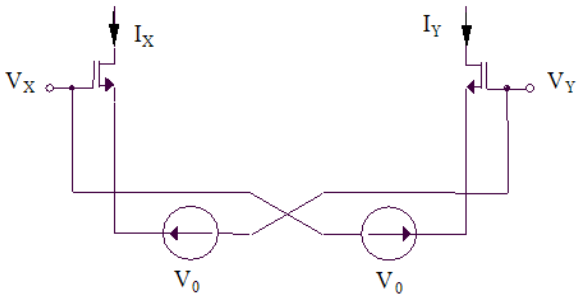

Fig. 1. The CMOS differential amplifier based on the constant sum of gate-source voltages.

Considering a saturation biasing of the two MOS transistors from Fig. 1, the I_X and I_Y currents will have the following expressions:

$$I_X = \frac{K}{2}\left[(V_X - V_Y) + (V_O - V_T)\right]^2, \tag{1}$$

$$I_Y = \frac{K}{2}\left[-(V_X - V_Y) + (V_O - V_T)\right]^2, \tag{2}$$

resulting a linear dependence of the differential output current on the differential input voltage, equivalent with a constant circuit transconductance g_m:

$$I_X - I_Y = g_m\,(V_X - V_Y)\,, \tag{3}$$

where:

$$g_m = 2K\,(V_O - V_T)\,. \tag{4}$$

The only important disadvantage of this general implementation of the differential amplifier is that the transconductance is function on the threshold voltage of the MOS devices. So, considering the second-order effects that appear in the MOS transistor operation, the circuit linearity will be affected by the bulk effect. The original idea to overcome this problem is to use instead independent voltage sources V_O two controlled voltage sources, practical implemented using two gate-sources of MOS transistors biased in saturation. In this case, the equivalent circuit transconductance will be obtained replacing in (4) the expression $V_O = V_T + \sqrt{2I_O/K}$, I_O being the biasing current of the MOS transistors from the controlled voltage sources. It results:

$$g_m = 2\sqrt{2KI_O}. \tag{5}$$

A possible implementation in CMOS technology of the previous differential amplifier, having the important advantages of a very large input impedance and of a relatively simplicity is presented in Fig. 2. The equivalent transconductance of the proposed implementation is given by $g_m = 2K\,(V_C - V_T)$, V_C being a voltage which allows to control g_m. In order to avoid the linearity degradation caused by the bulk effect (V_T appears in the expression of g_m even in the case of implementing the voltage

sources V_0 from Fig. 1 as gate-source voltages because the transconductance of the circuit is voltage-controlled, not current-controlled), an improved realization of the circuit is presented in Fig. 3. In this case, the voltage sources V_0 are implemented as a sum of two gate-source voltages ($T_3' - T_3''$ and $T_4' - T_4''$, respectively).

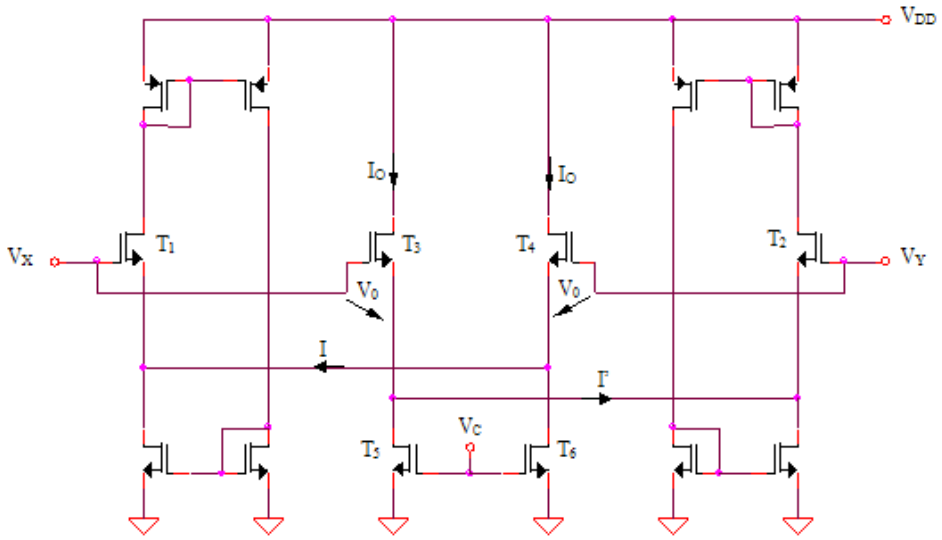

Fig. 2. The implementation in CMOS technology of the differential amplifier based on the constant sum of gate-source voltages.

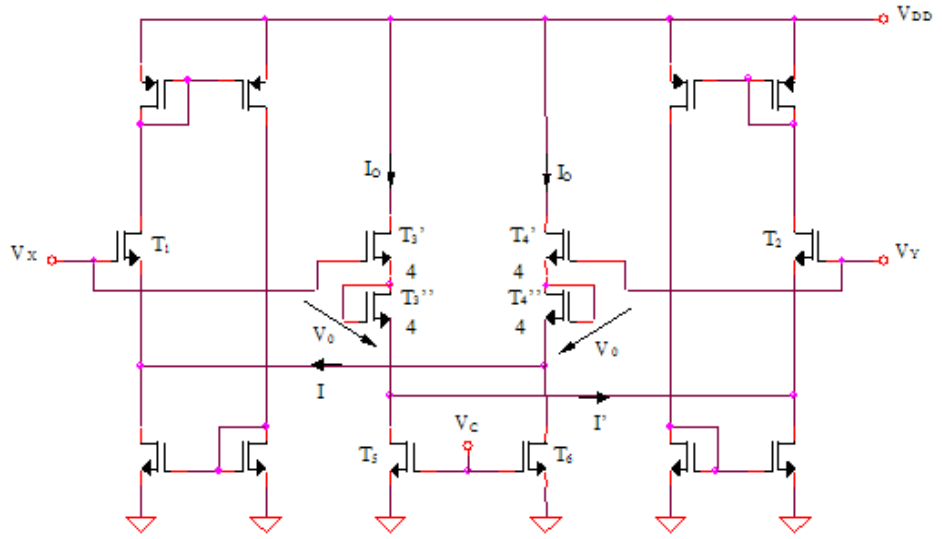

Fig. 3. The implementation of the differential amplifier with improved linearity.

2.1.2. The second-order effects

The relation (5) is given for a perfect quadratic characteristic of the MOS transistor biased in saturation region, in practice it being slightly modified by the second-order effects, modeled by the following relations: channel-length modulation (6) and mobility degradation (7)).

$$I_D = \frac{K}{2}\left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right) \tag{6}$$

$$K = \frac{K_0}{\left[1 + \theta_G (V_{GS} - V_T)\right]\left(1 + \theta_D V_{DS}\right)} \tag{7}$$

Taking into account these second-order effects and considering that the design condition $\lambda = \theta_D$ is fulfilled, the operation of the differential amplifier from Fig. 1 will be affected by a small error that will be further quantitative evaluated.

Considering the second-order effects, relations (1) and (2) must be rewritten as:

$$I_X = \frac{K}{2}\left(V_{GSX} - V_T\right)^2 \frac{1}{1 + \theta_G\left(V_{GSX} - V_T\right)}, \tag{8}$$

$$I_Y = \frac{K}{2}\left(V_{GSY} - V_T\right)^2 \frac{1}{1 + \theta_G\left(V_{GSY} - V_T\right)}, \tag{9}$$

resulting, after some approximations, that the differential amplifier operation will be affect by third-order distortions as a result of second-order effects:

$$I_X - I_Y = a_1\left(V_X - V_Y\right) + a_3\left(V_X - V_Y\right)^3, \tag{10}$$

where a_1 and a_3 are constants coefficients having the following expressions:

$$a_1 = 2K\left(V_O - V_T\right) - 3K\theta_G\left(V_O - V_T\right)^2,$$

$$a_1 \cong 2K\left(V_O - V_T\right) = 2\sqrt{2KI_O}, \tag{11}$$

and:

$$a_3 = K\theta_G. \tag{12}$$

The quantitative evaluation of these distortions could be made computing the total harmonic distortion coefficient:

$$THD_1 \cong \frac{a_3\left(V_X - V_Y\right)^3}{a_1\left(V_X - V_Y\right)} = \frac{\theta_G\left(V_X - V_Y\right)^2}{2\left(V_O - V_T\right)}. \tag{13}$$

2.1.3. The linearization technique for the CMOS differential amplifier

An original method for linearizing the transfer characteristic of the differential amplifier from Fig. 1, even in the worst case of considerring the second-order effects

modeled by (6) and (7) is to use an anti-parallel connection of two quasi-identical differential structure, different biased ($I_{O1} \neq I_{O2}$) and opposite excited. Re-writing the expression (10) of the differential output current for these two differential amplifiers, it results:

$$(I_X - I_Y)^1 = a_1^1 (V_X - V_Y) + a_3^1 (V_X - V_Y)^3 , \tag{14}$$

$$(I_X - I_Y)^2 = a_1^2 (V_X - V_Y) + a_3^2 (V_X - V_Y)^3 , \tag{15}$$

where $a_1^1 \cong 2\sqrt{2KI_{O1}}$, $a_1^2 \cong 2\sqrt{2KI_{O2}}$ and $a_3^1 = a_3^2 = K\theta_G$. The total expression of I_{XY} current obtained considerring this anti-parallel connection is given by the difference between the individual currents (14) and (15):

$$I_{XY} = (I_X - I_Y)^1 - (I_X - I_Y)^2 . \tag{16}$$

Combining the previous relations, it results a linear transfer characteristic of the anti-parallel differential amplifier, even taking into account the second-order effects that affect the MOS transistor operation:

$$I_{XY} = g_m (V_X - V_Y) , \tag{17}$$

the transconductance g_m having the following expression:

$$g_m = 2\sqrt{2K} \left(\sqrt{I_{O1}} - \sqrt{I_{O2}} \right) . \tag{18}$$

2.2. The implementation of the CMOS active resistor with positive equivalent resistance

A small changing in Fig. 1 allows to obtain a circuit that simulates a linear current-voltage characteristic, so an active resistor circuit.

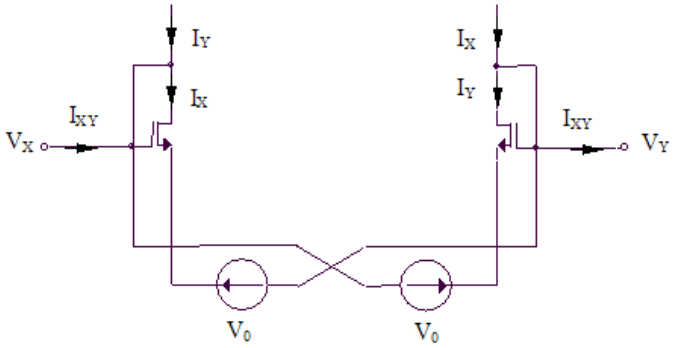

Fig. 4. The active resistor derived from the differential amplifier structure.

Using the same relations, the current $I_{XY} = I_X - I_Y$, which is passing through the input pins of the active resistor, V_X and V_Y will be given by (3). So, the equivalent resistance of the circuit presented in Fig. 2 could be defined as:

$$R_{ECH} = \frac{V_X - V_Y}{I_{XY}} = \frac{1}{g_m} = \frac{1}{2\sqrt{2KI_O}}. \tag{19}$$

Besides its simplicity, another great advantage of the proposed implementation of the active resistor proposed in Fig. 4 is the possibility of a very facile control of the value of the equivalent resistance by changing the current I_O. A possible implementation in CMOS technology of the principle briefly described in the previous lines is presented in Fig. 5.

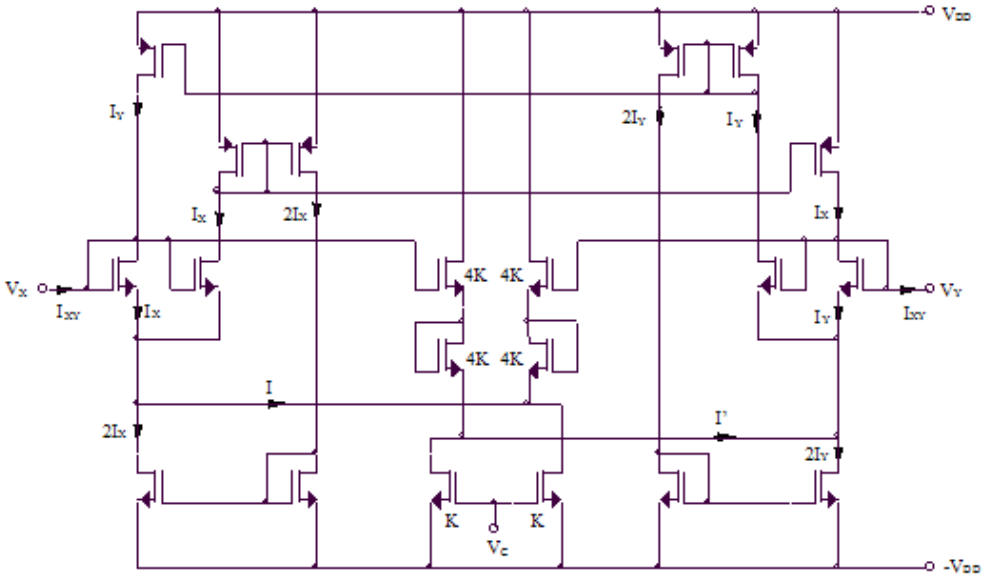

Fig. 5. The implementation in CMOS technology of the general principle shown in Fig. 4.

2.3. The implementation of the CMOS active resistor with negative equivalent resistance

Starting from the active resistor with positive equivalent resistance presented in Fig. 4, in order to obtain a circuit with a controllable negative equivalent resistance circuit, the original idea is to use the following shown cross-connection, resulting the circuit presented in Fig. 6.

The equivalent resistance of the circuit from Fig. 6 is:

$$R'_{ECH} = -R_{ECH} = -\frac{1}{2\sqrt{2KI_O}}. \tag{20}$$

The area of applications of controllable negative resistance active resistors covers many domains, including the canceling of amplifiers' gain load or the design of improved performances integrators.

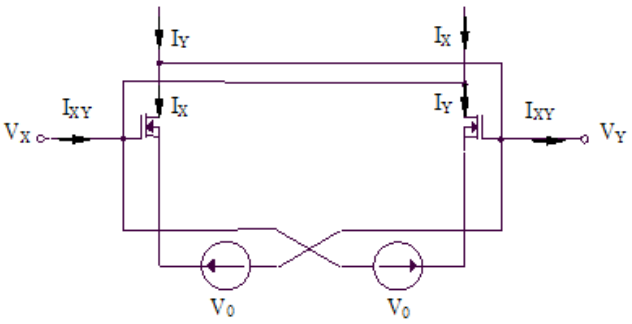

Fig. 6. The controllable negative resistance active resistor.

3. Simulated results

The CMOS active resistor with positive resistance from Fig. 4 was implemented in 0.35 μm CMOS technology. The estimated characteristic $(I_1 - I_2)(V_X - V_Y)$ is presented in Fig. 7.

The maximum linearity error of the active resistor for a reduced value of the supply voltage, $V_{DD} = \pm 3$ V and a limited input voltage range ($|V_X - V_Y| \leq 500$ mV) is smaller than a percent.

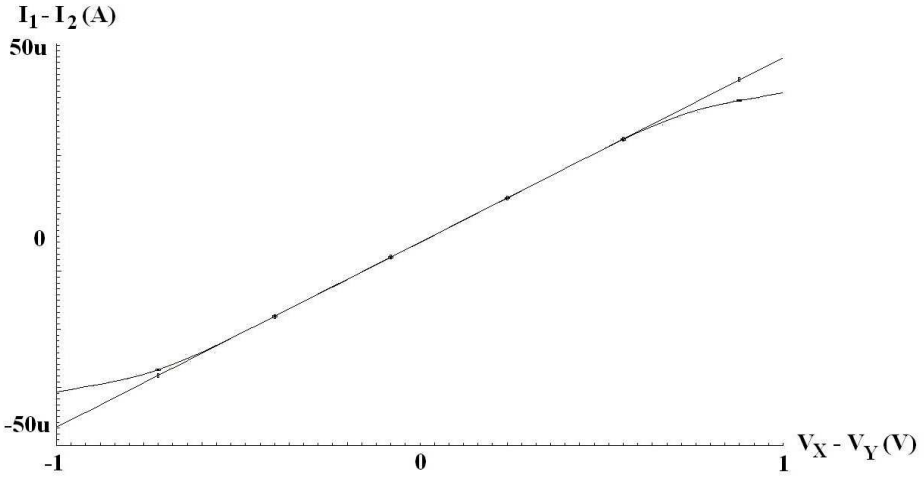

Fig. 7. The estimated characteristic.

4. Conclusions

An original multifunctional structure with improved performances has been presented. The core of the circuit is represented by a differential amplifier based on an original linearization technique. The great advantages of the increased modularity and controllability and of the reduced design costs associated represent an immediate consequence of the multiple functions realized by the proposed structure: amplifying, multiplying or simulating positive and negative resistances. The frequency response and the linearity have been strongly increased by implementing original techniques, while the silicon area per function has been reduced as a result of the multifunctionality. The SPICE simulation confirms the theoretical estimated results, showing a linearity error less than a percent for a small value of the supply voltage ± 3 V and for an extended input range ± 500 mV.

References

[1] WANG Z., *Current-controlled Linear MOS Earthed and Floating Resistors and Application*, *IEEE Proceedings on Circuits, Devices and Systems*, pp. 479–481, 1990.

[2] SELLAMI L., *Linear Bilateral CMOS Resistor for Neural-Type Circuits*, *Proceedings of the 40^{th} Midwest Symposium on Circuits and Systems*, vol. **2**, pp. 1330–1333, 1997.

[3] SINGH S.P., HANSOM J.V., VLACH J., *A New Floating Resistor for CMOS Technology*, *IEEE Transactions on Circuits and Systems*, pp. 1217–1220, 1989.

[4] SAKURAI S., ISMAIL M., *A CMOS Square-law Programmable Floating Resistor*, *IEEE International Symposium on Circuits and Systems*, pp. 1184–1187, 1993.

[5] PAPAZOGLOU C.A., KARYBAKAS C.A., *Electronically Tunable Floating CMOS Resistor Independent of the MOS Parameters and Temperature*, *Proceedings of Electronics, Circuits and Systems, The 6^{th} IEEE International Conference on ICECS*, pp. 311–314, 1999.