ROMANIAN JOURNAL OF INFORMATION SCIENCE AND TECHNOLOGY
Volume **11**, Number 2, 2008, 193–202

Application of the LTCC Technology for the Fabrication of the RF 3D Inductor

G. RADOSAVLJEVIĆ[1], A. MARIĆ[1], G. STOJANOVIĆ[1], L. ŽIVANOV[1], W. SMETANA[2], M. UNGER[2], H. HOMOLKA[2]

[1] Faculty of Technical Sciences, University of Novi Sad, Trg Dositeja Obradovića 6, Novi Sad, Serbia

E-mail: rgoran@uns.ns.ac.yu

[2] Institute for Sensor and Actuator Systems, Vienna University of Technology, Gushausstrasse 25-29, Vienna, Austria

Abstract. This paper introduces implementation of the LTCC technology in fabrication of multilayer inductors. Easy fabrication of 3D structures offers a comfortable way for the miniaturization of passive components, since their small dimensions are required in RF applications. A novel design of multilayer inductor is presented and its characteristics compared to the planar structure with same geometrical parameters. It is shown that 3D structure displays better behaviour in the frequency range of interest. Also, fabrication steps of the LTCC technological process are presented on the example of the projected inductor.

Key words: LTCC technology, multilayer structures, RF inductor.

1. Introduction

The fabrication of microinductors can employ various microsystem technologies. The choice of the adequate technology depends on overall dimensions of the designed component, its performance and application area. When speaking of the most widely spread technologies used for the fabrication of microinductors, it is mainly referred to the monolithic [1–3], the thick film (TF) [4–6] and the LTCC (Low Temperate Co-fired Ceramic) [7–9] technology.

The monolithic technology is appropriate for the fabrication of miniature inductors (200 μm overall dimension). But, monolithic inductors have smaller value of the inductance and quality factor (Q-factor) in comparison to similar structures realized in the LTCC technology.

The TF technology is often employed for the realization of microelectronic components and circuits. It implies low operating temperatures (between 850°C and 1000°C) and therefore is suitable for the implementation of good conductors. However, the TF method involves multiple firing of lower layers which results in changed characteristics of used pastes and thus diminished properties of final components.

The LTCC technology can be defined as the lamination of several ceramic tapes at a low temperature. The fabrication of components in the LTCC technology involves application of various pastes on a single ceramic tape and later superposition of tapes into a stacked structure [10]. Pastes can be made of conductive, dielectric or resistive material depending on the type of the component that is being fabricated.

One advantage of this technology is the possibility of testing each layer separately, avoiding the need for re-fabrication of the whole structure in case of an error or inaccuracy. The problem of multiple firing present in the TF method does not appear in the LTCC technology since it implies co-firing of all layers. Having in mind the low operating temperature (below 1000°C), standard thick films of gold, silver or platinum as conductive materials can be used in this process. Thick films of materials leave the possibility of placing individual electronic components on the structure together with the network of conductors enabling assembly of multi-chip modules.

The LTCC technology can find its way in many applications. It can be used for manufacturing planar components, yet its main usage is for the multilayer structures. It is commonly present in fields that involve the work in extreme conditions (at high temperatures and humidity), micro- and milli- waves, wireless communication modules, radio frequency (RF) passive components such as inductors, capacitors, resonators, filters, baluns, antennas, high precision multiple chip modules, navigation equipment, etc. [11, 12].

This paper introduces the LTCC technology as a suitable method for the fabrication of multilayer inductors. Fabrication steps are showed on the example of one multilayer inductor (3D inductor). The comparison of characteristics of the planar (single conductive layer) and the 3D (multi conductive layer) inductor is also made in order to demonstrate benefits of the multilayer design.

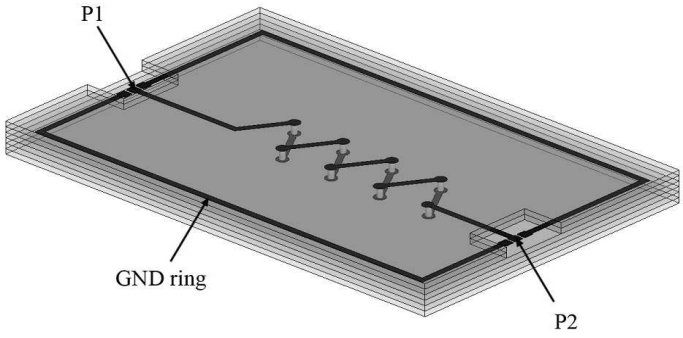
2. The fabrication proces

The fabrication process in the LTCC technology involves implementation of the following steps:

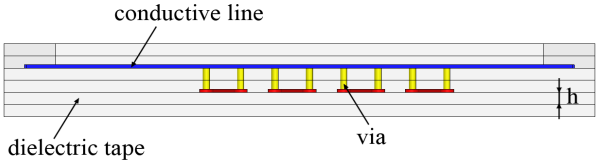
– designing masks for vias and cutting tapes with a laser,
– designing masks for the application of conductive pastes,
– cutting outline and drilling holes in tapes with a laser,
– fine line printing of conductive pastes and via filling by stencil printing,
– additional cleaning of every layer,

– alignment of tapes and stack formation,
– lamination, firing and verification,
– dicing of tapes to single elements.

Each of these steps will be explained on the example of the buried 3D inductor illustrated in Fig. 1. Symbols P1 and P2 in Fig. 1a represent used ports and GND ring stands for the ground line that rounds the structure. In the Fig. 1b the cross-section of the inductor is shown, with indicators for interconnections between conductive layers (via), dielectric tapes and their thickness (h) and conductive lines. Outer dimensions of this inductor are $(8 \times 5 \times 0.564)$ mm. The width of conductive strips is 100 μm. There are six layers (tapes) all together that form the whole structure.



a) the 3D inductor



b) cross-section of the 3D inductor

Fig. 1. View of the 3D inductor.

Table 1. Parameters for Heraeus Heratape®CT 700-5.1-267

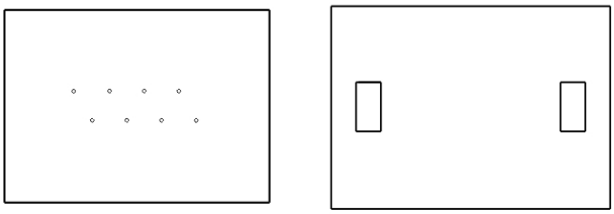
Heraeus Heratape®CT 700-5.1-267	
Dielectric constant for the (1÷10) GHz range	6.6
Tape thickness, h (μm)	130
Shrinkage along x- and y- axis (%)	14.9
Shrinkage along z-axis (%)	28.4

The inductor itself is placed in the second, the third and the fourth layer. Used dielectric tapes are produced by the company Heraeus [13], model name Heratape CT 700-5.1-267. Their main properties are given in Table 1. The material used for conductive layers is from the same manufacturer; silver under the label TC 7305

and TC 7304 is used for conductive lines and vias, respectively. These materials are compatible with the one used for dielectric tapes, which means that they have the same shrinkage coefficient along x- and y- axis.

The fabrication of components that use the LTCC technology requires designing of two different types of masks. One type is needed for vias and for cutting (masks for cutting, data file) and the other is used for the application of conductive pastes (masks for films, photomask).

Masks can be designed in one of the CAD oriented programs (for example AutoCad®, P-Cad®, LTCC Layout Editor®, etc.). Masks used for inductors presented in this paper are designed in AutoCad. The layout of masks for vias and for the cutting is done for each layer separately. A designer should bear in mind shrinkage of the material during the firing process. Therefore, dimensions of designed masks should be greater than dimensions of the projected structure for the value of the shrinkage. Figure 2 shows masks for vias and for contacts used for the laser.



a) the mask for vias b) the mask for contacts

Fig. 2. Designed masks for the laser.

For the first two layers no mask is required, because the inductor is placed in higher layers. The mask used for the third and fourth layer is designed for vias, Fig. 2a). Holes for vias must be smaller then via pads placed on the mask for films in order to obtain good alignment of the mask and the tape. This difference in size should be minimally 50 μm regarding the hole diameter. Masks for the fifth and sixth layer should provide contacts for the measuring probes, Fig. 2b).

A mould should be used to achieve the accurate superposition of tape layers. Mould dimensions are (48 × 28) mm. If they are compared to dimensions of the designed inductor, plenty of unused space can be observed on the plate. Therefore, three more inductor structures are designed and placed on the same plate.

Drilling holes and cutting outlines is done with a laser. NdYAG laser is typically used in this procedure. Laser machining is conducted by computer-controlled galvosystem. Laser machining parameters have to be adjusted to the selected tape type and thickness. If parameters are not adequately set holes may not be completely punctured or tape edges may not be smooth. After the cutting process some holes could still be closed due to the appearance of glass particles formed while cutting. If there are some particles left, they can be eliminated by using compressed air (for example). Figure 3 shows the cutting process realized with the NdYAG laser.

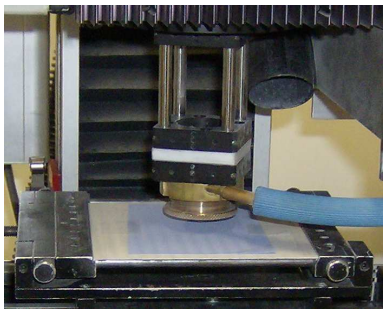


Fig. 3. The cutting process.

Tapes obtained after the cutting process are presented in Fig.4.

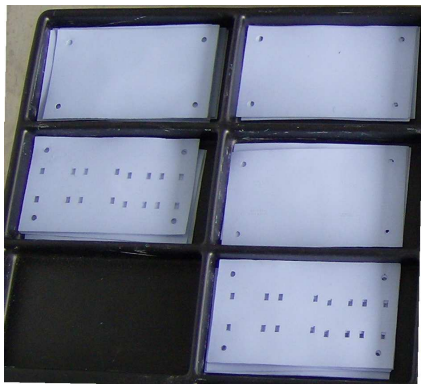


Fig. 4. Tapes after the cutting process.

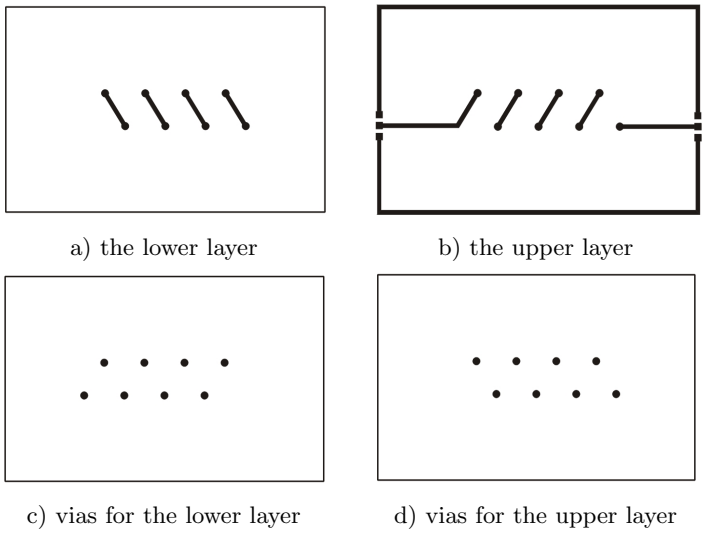
Masks for the application of conductive pastes onto tapes are also designed for each layer separately. Their dimensions must be corrected due to the shrinkage present after the firing. Masks for conductive layers and vias are presented in Fig. 5.

After masks are designed they must be fabricated by printing the design onto the foil and its later transfer onto the photo-paper. When the photomask is ready conductive layers can be screen-printed onto tapes.

The application of conductive layers is done using the screen-printing procedure. This procedure is not very reliable for the filling up via holes due to the imprecide overlapping of the mask and the tape. The diameter of via holes is 100 μm and the number of holes on the one tape is between five and ten for designed inductors. If aligning is not ideal, the holes and the mask will not match correctly. Therefore, via filling is conducted with the stencil printing procedure.

The superposition of tapes is done on the mould. When each tape is placed into the mould, lamination is done under the pressure of 50 kN and 65°C temperature. It is followed with firing done in the oven at the temperature of 867°C, in total duration of five hours. The laminated structure is placed onto conveyor and pulled into the oven. The high firing temperature can cause bending or breakage of tapes due to unequal shrinkage of tapes and pastes. Thus, laminated tapes are covered with a

special tape for protection. Figure 6 shows the plate with designed structures at the end of the fabrication process.



a) the lower layer b) the upper layer

c) vias for the lower layer d) vias for the upper layer

Fig. 5. Designed masks for conductive layers.

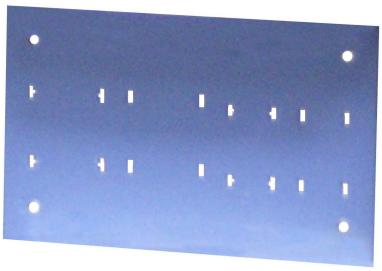
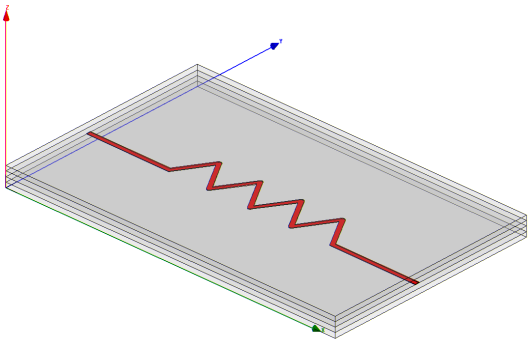


Fig. 6. The fabricated plate.

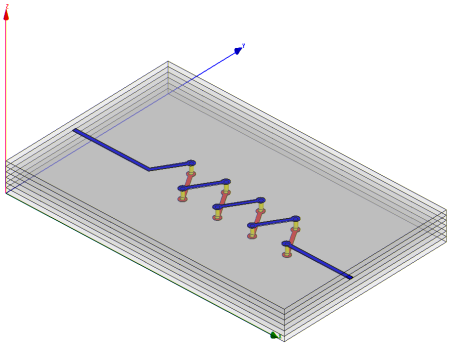
3. Simulation results of the planar and the 3D inductor

Models of the designed planar and 3D inductor are presented in Fig. 7. Inductors are designed to have the same number of segments, the same width and to occupy the same area on the plate.

These models have been simulated using the electromagnetic simulator Ansoft HFSS [14]. The main geometrical and technology parameters of the ceramic tape and conductive paste used in simulations are given in Table 2. It is important to notice that in geometrical parameters (the thickness of tape and conductive lines) shrinkage present after firing is accounted.



a) the planar inductor



b) the 3D inductor

Fig. 7. Designed inductor structures as modeled in Ansoft HFSS.

Table 2. Simulation parameters for tape and paste

	Tape	Paste
Relative permittivity	6.6	1
Relative permeability	1	0.9998
Thickness (μm)	94	10
Bulk conductivity (S/m)	/	$6.1 \cdot 10^6$

Simulation results of these structures are presented in Figs. 8 and 9, showing dependence of the inductance and the Q-factor on the frequency.

Obtained inductances are 6.17 nH for the planar inductor and 7.79 nH for the 3D inductor at 1 GHz operating frequency. As it was expected, a higher value of inductance has been achieved for the 3D inductor. This increase can be explained with an additional inductance that comes from vias present in the 3D configuration.

More important improvement of the 3D configuration compared to the planar structure can be seen through the significant increase of the quality factor in the whole frequency range of interest. While the planar inductor has the value of the Q-factor 61 at 1 GHz, the Q-factor of the 3D inductor goes up to 72 at the same frequency.

Increase of the inductance and the quality factor value of the 3D inductor illustrate one of the advantages of multilayer structures fabricated in the LTCC technology compared to the planar design with similar geometrical and technological parameters.

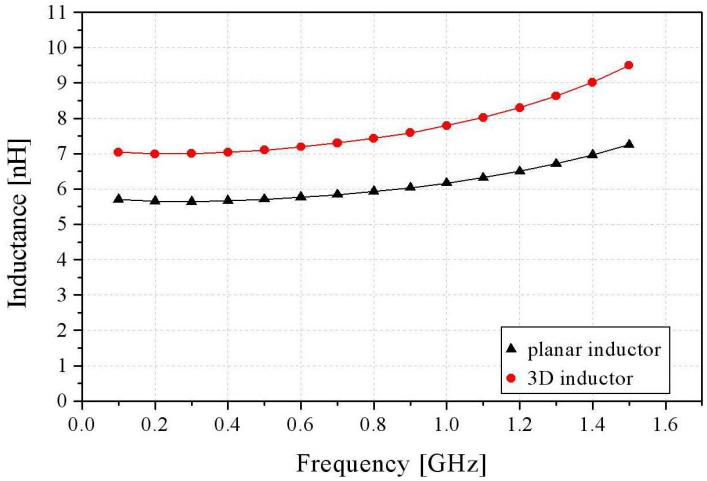


Fig. 8. The inductance versus frequency.

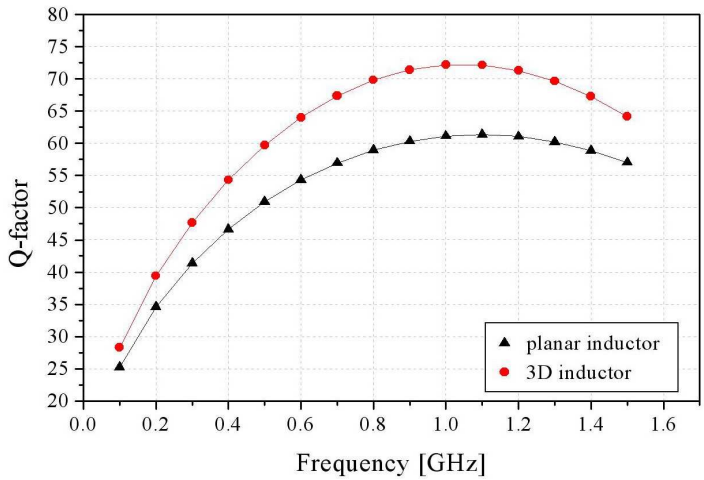


Fig. 9. The Q-factor versus frequency.

4. Conclusions

The LTCC technology introduces some novelties and improvements in the fabrication process of microelectronic components and circuits. The implementation of the LTCC technology allows easy fabrication of different RF passive components. Due

to the possibility of the parallel processing larger number of components can be fabricated onto same plate achieving higher productivity in comparison to the standard thick film technology. Fabrication steps can be automatized and therefore made suitable for the serial production. With the increase of operating frequencies and decrease of dimensions of electronic devices, good characteristics of LTCC materials can put this technology in the leading position in the micro-fabrication industry. It has been showed that the multilayer structure has higher value of the inductance and the quality factor compared to the planar structure with similar geometrical and technological parameters, presenting in that manner some advantages of the LTCC technology.

Acknowledgement. This work is supported by the project INCO-CT-2006-043669-ReCIMICo.

References

[1] NIKNEJAD A. M., MAYER R. G., *Analysis, design, and optimization of spiral inductors and transformers for* Si *RF IC's*, IEEE Journal of Solid- State Circuits, vol. **3**, no. 10, pp. 1470–1481, Oct. 1998.

[2] KOUTSOYANNOPOULOS Y. K., PAPANANOS Y., *Systematic analysis and modeling of integrated inductors and transformers in RF IC design*, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. **47**, no. 8, pp. 699–713, Aug. 2000.

[3] LONG J. R., *Monolithic transformers for silicon RF IC design*, IEEE Journal of Solid-State Circuit, vol. **35**, no. 9, pp. 1368–1382, Sept. 2000.

[4] DESNICA V., ŽIVANOV L., ALEKSIĆ O., JENEI S., *Modeling and optimization of thick film solenoid-bar type inductors and transformers*, COMPEL, vol. **19**, no. 2, pp. 615–621, 2000.

[5] ARSHAK K. I., ALMUKHTAR B., *Development of high frequency coreless transformer using thick film polymer technology*, Microelectronics Journal, **30**, pp. 119–125, 1999.

[6] O'REILLY S., FLANNERY J., O'DONNELL T., MUDDIMAN A., HEALY G., BYRNE M. L., Ó MATHÚNA S. C., DUFFY M., HURLEY G., *A comparative analysis of interconnection technologies for integrated multilayer inductors*, Microelectronics International, vol. **15**, no. 1, pp. 6–10, 1998.

[7] GOLONKA J., *New application of LTCC technology*, 28^{th} Int. Spring Seminar on Electronics Technology, pp. 148–152, 2005.

[8] GOLONKA L. J., Technology and applications of Low Temperature Cofired Ceramic (LTCC) based sensors and mycrosystems, Bulletin of the Polish Academy of Sciences, Technical Sciences, vol. **54**, no. 2, pp. 221–231, 2006.

[9] MÜLLER J., *High-quality RF inductors in LTCC*, ISHM'96 Conference, Minneapolis, October, 1996.

[10] *LTCC Design Guide*, Formosa Teletek Corporation, 2004.

[11] MARIĆ V., ŽIVANOV L., STOJANOVIĆ G., *RF and MEMS components in LTCC Technology*, 6^{th} Int. Symp. on Interdisciplinary Regional Research - (Hu – Ro – Yu), pp. 208–213, Novi Sad, October, 2002.

[12] GUO Y-X., ZHANG Z.Y., ONG L.C., CHIA M.Y.W., *A novel LTCC miniaturized dualband balun*, IEEE Microwave and Wireless Components Letters, vol. **16**, no. 3, pp. 143–145, 2006.

[13] `www.heraeus.com`

[14] *Ansoft Inc. HFSS (High Frequency Structure Simulator)*, Pittsburg: Ansoft Corporation, 2002.