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Oscillator Based on Suspended Gate MOS Transistors

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Abstract. The paper deals with the oscillator applications based on vibrating mode of the suspended gate SG-MOSFET transistor. In order to simulate the electrical behavior of the transistor a small-signal equivalent circuit of the gate is proposed and validated. An adapted 16MHz oscillator topology originated from Pierce scheme is demonstrated.

1. Introduction

Suspended gate MOS-FET (SG-FET) transistors involve a suspended metal membrane [1] over the channel region of a solid state MOS-FET (Fig. 1).

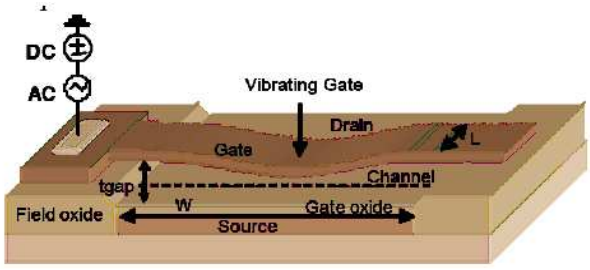

Fig. 1. A schematic view of SG-FET.

SG-FET resonators have been demonstrated to have great potential for CMOS co-integrated reference oscillator applications [2]. The main advantages of these resonators are rather high quality factor, large output current and CMOS co-integrability [3]. One of the main application using resonators consists in providing a stable and

precise time reference. Nowadays, this is realized by quartz resonators, that provides a very stable frequency but are big and off chip (not integrable). The SG-FET based oscillators can potentially offer different resonant frequencies on the same chip, due to the dependence of these frequencies on the design (dimensions) of suspended gate. Full CMOS integration and possibility of multi-frequency in the same process make, in general, the MEMS resonator serious candidates for replacing quartz.

2. Static and dinamic regime

One of the biggest problems of MEMS resonators is the output current that is very small, especially for scaled structures. To overcome this problem, the conventional capacitive detection is replaced by a MOS detection when the vibrating gate modulates the MOSFET drain current [4].

As the gate voltage is increasing, the gate is approaching the oxide and at one third of the gap, it collapses. This is due to the loss of the equilibrium condition between the electrostatic force and the elastic one. This voltage (pull in voltage) can be calculated [5] as:

$$V_{pi} = \sqrt{\frac{8kd^3}{27\varepsilon_0 A}}, \tag{1}$$

where k is the stiffness of the gate, d – the air gap, A – the area of the gate over the channel and ε_0 – the permittivity of the free space.

For a proper linear resonance, SG-MOSFET should be biased at a lower voltage.

To use this transistor as a resonator, first a convenient bias is applied and over it, a sinusoidal signal. The transfer function has a maximum at the resonating frequency that depends only on the material dimensions and properties. One big disadvantage is that the quality factor is strongly limited by air damping hence a vacuum package is necessary.

Based on the mechanical equations, an equivalent electrical circuit of the gate is conceived. First the vibrating gate is considered, mechanically speaking, as a plate that is suspended with a spring, having the movement equation:

$$m\ddot{Z} + b\dot{Z} + kZ = F, \tag{2}$$

where m is the effective mass of the beam, b – the dumping factor, k – the stiffness of the vibrating gate, F – the electrostatic force and Z – the elongation. The resonating frequency of the beam is given by:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k}{m}}. \tag{3}$$

The mechanical movement determines electrical charge variations on the gate and, consequently, electrical oscillations. The electrical regime of this vibrating gate can be analyzed with an equivalent circuit.

3. Small-signal regime of the vibrating gate

The SG-MOSFET is a conventional MOS transistor that has as gate the outer surface of the oxide – named internal gate (G_{int}) – and is serially coupled with an air capacitor (C) between G_{int} and G, as is shown in Fig. 2.

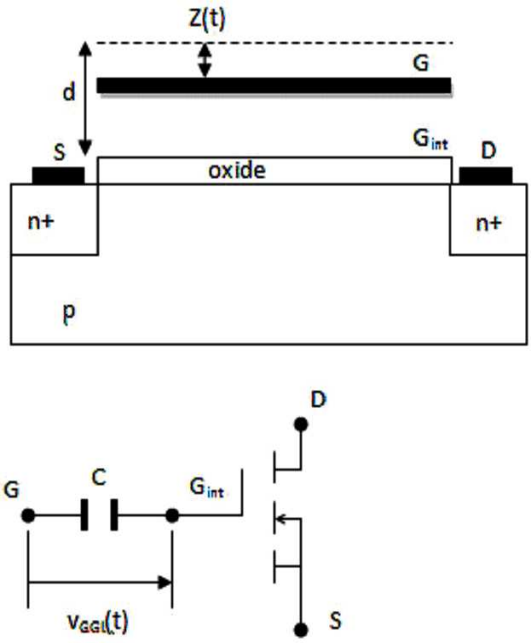

Fig. 2. The SG-MOSFET as a conventional MOS transistor with internal gate G_{int} in series with the air capacitor C.

In the absence of the gate bias, the gap between gate and oxide is d; applying a voltage on the gate, the mobile electrode G is attracted toward the oxide with a distance Z. In this way, the value of the air capacitor C is given by:

$$C = \frac{\varepsilon_0 A}{d - Z}. \tag{4}$$

The displacement Z is obtained from the movement equation (2) where the electrostatic force is:

$$F = \frac{\varepsilon_0 A v_{GGi}^2}{2(d - Z)^2}. \tag{5}$$

The voltage v_{GGi} is the part of the gate voltage v_G, effectively applied to the air capacitor (see Fig. 2).

The vibrating mode of the gate is obtained biasing this electrode with a d.c. voltage in series with a low amplitude sinusoidal signal; in this way:

$$v_{GGi}(t) = V_{GGi} + u(t), \tag{6}$$

where:

$$u(t) = U \sin \omega t \quad \text{with} \quad U \ll V_{GGi}. \tag{7}$$

The small-signal condition permits to approximate the term v_{GGi}^2, from equation (5), as:

$$v_{GGi}^2 = (V_{GGi} + u(t))^2 \approx V_{GGi}^2 + 2V_{GGi}u(t), \tag{8}$$

and to separate the constant component from the variable one of the force F, resulting by applying eq. (8) to eq. (5):

$$F \approx \frac{\varepsilon_0 A V_{GGi}^2}{2(d-Z)^2} + \frac{\varepsilon_0 A V_{GGi} u(t)}{(d-Z)^2}. \tag{9}$$

The displacement $Z(t)$ has the same behavior:

$$Z(t) = Z_0 + z(t), \tag{10}$$

where the constant term Z_0 is the result of the d.c. voltage V_{GGi}, while $z(t)$ is generated by $u(t)$. The same inequation occurs:

$$z(t) \ll Z_0. \tag{11}$$

That permits to approximate eq. (4) as follows:

$$C(t) = C_0 \left[1 + \frac{z(t)}{d - Z_0}\right], \tag{12}$$

where C_0 is the static value of the capacitor:

$$C_0 = \frac{\varepsilon_0 A}{d - Z_0}. \tag{13}$$

Introducing the eqs. (9) and (10) in the movement equation (2) it can be separated the two ways for the calculations of the Z_0 and $z(t)$. For Z_0 the following equation is obtained:

$$kZ_0 = \frac{\varepsilon_0 A V_{GGi}^2}{2(d - Z_0)^2}, \tag{14}$$

that represents a known result for the case of a d.c. gate voltage applied. In order to obtained the "vibrations" $z(t)$ the specific movement equation is given by:

$$m\ddot{z} + b\dot{z} + kz = \frac{\varepsilon_0 A V_{GGi} u}{(d - Z_0)^2}. \tag{15}$$

It can be observed that the dynamic regime is described by a separate equation, but is depending of the static regime, via V_{GGi} and Z_0. This observation explains the possibility of oscillation control by static regime.

4. Equivalent small-signal circuit of the gate

The equivalent circuit of the gate starts with the gate current calculation, $i(t)$, as is shown in Fig. 3.

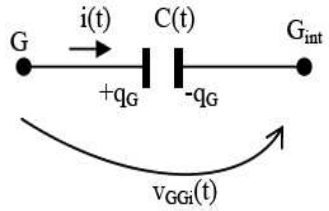

Fig. 3. The electrical regime of the variable air capacitor, $C(t)$.

The current through capacitor appears due the variable charges, q_G, on its plates; these charges are generated by the variable capacitance $C(t)$ determined by variable air gap $d - z(t)$ and the variable applied voltage, $v_{GGi}(t)$. As result:

$$i(t) = \dot{q}_G = \frac{\mathrm{d}}{\mathrm{d}t}\left[C(t)v_{GGi}(t)\right] = \dot{C}(t)v_{GGi}(t) + C(t)\dot{v}_{GGi}(t) \approx \dot{C}(t)V_{GGi} + C_0\dot{u}(t). \quad (16)$$

The last approximations in the above equations take into account the specific conditions of the small-signal (6), (7) and (12). The equation (16) indicates that the equivalent circuit of the gate has two parallel branches, one given by the variable capacitance $C(t)$ and the other by the variable applied voltage $u(t)$, as it is shown in Fig. 4. The branch of the equivalent circuit directly related to the $u(t)$ is done by the C_0 capacitor, namely the static value of the air capacitor, determined by its static bias V_{GGi}.

In order to establish the other branch is important to have the dependence of the $\dot{C}(t)$ on applied voltage $u(t)$. For that, after the derivation of the equation (12), the dependence of $\dot{C}(t)$ on $\dot{z}(t)$ is obtained:

$$\dot{C}(t) = \frac{C_0}{d - Z_0}\dot{z}(t), \quad (17)$$

where permanent vibrations $z(t)$ are obtained in relation with $u(t)$ by solving the differential equation (15).

The equivalent circuit of this branch results in a series R_1, L_1, C_1 circuit (see Fig. 4). The capacitor C_1 is given by:

$$C_1 = C_0\frac{2Z_0}{d - Z_0}. \quad (18)$$

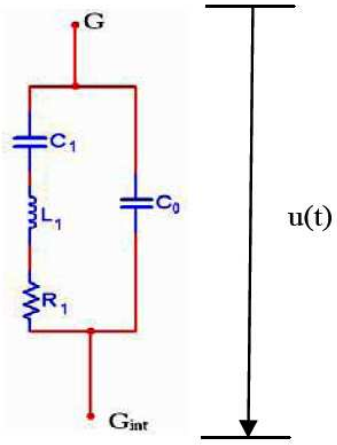

Fig. 4. The equivalent circuit of the vibrating gate.

The resonance of the series circuit L_1, C_1, R_1:

$$f_s = \frac{1}{2\pi\sqrt{L_1 C_1}} \tag{19}$$

is done by the mechanical resonance f_0 (3). Hence, the value of the inductor L_1 is obtained from:

$$L_1 = \frac{1}{2\pi^2 f_0 C_1}. \tag{20}$$

Regarding the equivalent circuit of the gate (Fig. 4), it can observe that electrical regime has an antiresonance, moreover than the mechanical one. The antiresonance frequency is given by:

$$f_d = \frac{1}{2\pi\sqrt{L_1 \dfrac{C_1 C_0}{C_1 + C_0}}}; \tag{21}$$

this frequency is greater than f_s.

5. Equivalent small-signal circuit of the transistor

The equivalent circuit of the SG-MOSFET is based on the observation shown in Fig. 2. The variable capacitor $C(t)$ is modeled by its equivalent circuit (figure 4), while the internal MOS transistor has a drain current that is proportional with the surface voltage (V_{gint}).

The equivalent circuit of the SG-FET is shown in Fig. 5.

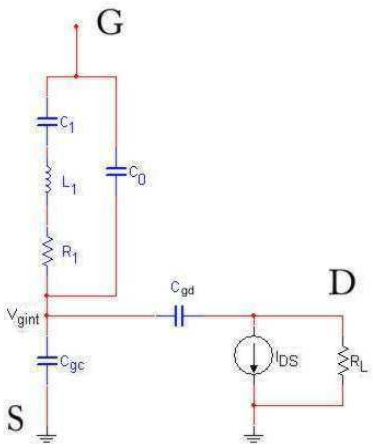

Fig. 5. Equivalent small signal circuit of the SG-FET.

They are introduced also C_{gd} that is the overlap capacitor and C_{gc} – the gate-substrate of the internal MOS.

Comparing the AC-analysis of the SG-FET with the one of the equivalent circuit, we obtain very similar curves (Fig. 6).

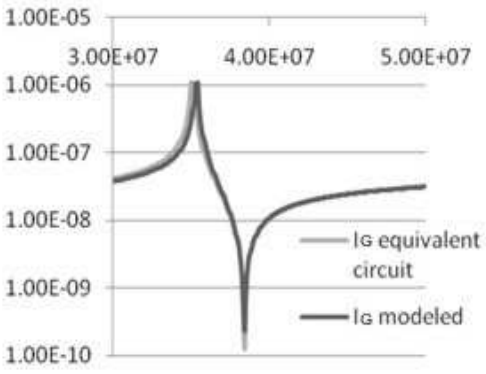

Fig. 6. AC analysis of gate current (gate current of the equivalent circuit and model.)

The analysis was made for a 35 MHz resonator.

6. Oscillator based on SG-FET

Based on the equivalent scheme of the SG-FET used in resonator (vibrating gate) mode, we propose to build an oscillator circuit. The device has the role of amplifying and offers a resonating circuit. A Pierce oscillator is chosen because of the capacitors that can be easily integrated in the CMOS technology and they present larger Q then the inductors. The gate is the resonating part and it is controlling the drain current.

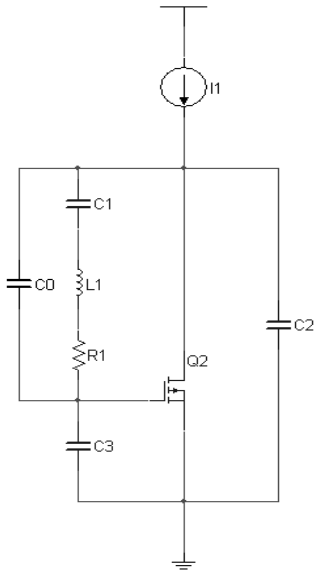

Fig. 7. Pierce oscillator scheme.

Comparing the schematics of a Pierce oscillator (Fig. 7) and the one with the small signal equivalent circuit of the SG-FET (Fig. 5), it is seen that the transistor has integrated almost all the parts of the oscillator and by connecting the gate with the drain, putting a proper bias and adding an external capacitor, the circuits are similar.

In this way the oscillator circuit is presented in Fig. 8.

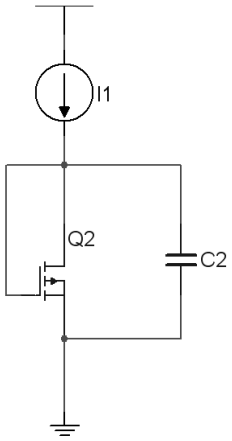

Fig. 8. SG-FET Oscillator scheme.

The components C_1, L_1, R_1, Q_2 and C_3 form the SG-FET, while C_2 is external. C_2 can also be another transistor of this type.

The R_1, L_1, C_1circuit should behave as an inductor (L_{eq}) for this circuit to oscillate. The AC behavior of a series RLC circuit in parallel with a capacitor is shown in Fig. 9.

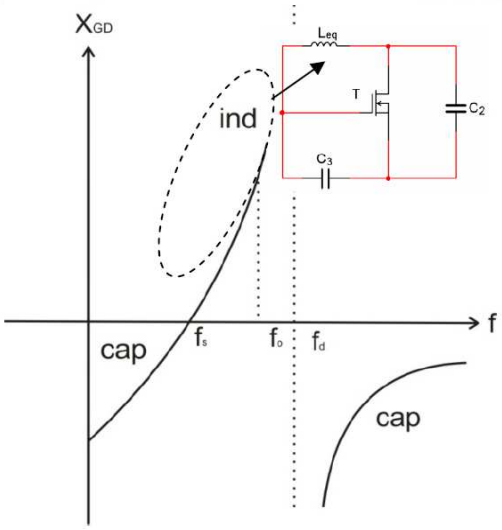

Fig. 9. AC behavior of the equivalent circuit corresponding to the Internal Gate - Drain circuit.

The resonating frequency of the system is between the resonating frequency of the gate and the antiresonance. If the circuit has a bigger Q then the antiresonance is coming closer to the resonance therefore the frequency is more stable.

The condition to starting the oscillations establishes the following inequality for the small-signal mutual conductance [8] g_{m0}:

$$g_{m0} > \frac{\omega}{QC_1}\frac{(C_2C_3 + C_2C_0 + C_3C_0)^2}{C_3C_2}, \tag{22}$$

which has a minimum if $C_2 = C_3$.

Losses in the circuit should be minimized to achieve minimum critical transconductance (and thus minimum current for oscillation) and maximum frequency stability. The maximum negative resistance is obtained for

$$g_m = g_{mopt} = \omega\left(C_3 + C_2 + \frac{C_3C_2}{C_0}\right) \tag{23}$$

and has the value

$$(-Re(Z_C))_{\max} = \frac{1}{2\omega C_3\left(1 + \dfrac{C_2 + C_3}{C_2C_3}C_0\right)}, \tag{24}$$

which must be larger than R_1 to allow oscillation.

7. Results and discussions

Based on a real device physical dimensions and materials, a 16 MHz [6] resonator has been simulated. The parameters correspond to a transistor with the length of the channel $L = 34$ µm, the width $W = 6$ µm, the length of the beam $L_{beam} = 30$ µm, the air gap 300 nm, and the oxide thickness $t_{ox} = 40$ nm. The gate was made out of aluminum-silicon alloy AlSi (1%) [7]. There were obtained oscillation with a frequency very close to the expected one. Figure 10 shows the oscillations obtained for drain voltage.

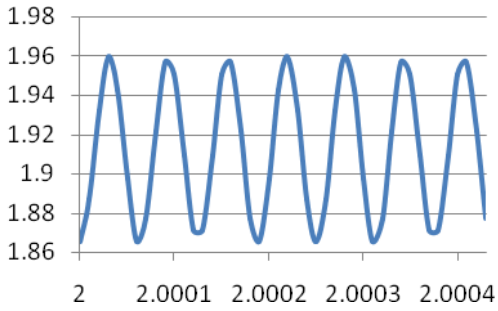

Fig. 10. Sinusoidal oscillations (drain voltage).

The electrical parameters of the oscillator and the dimensions of the suspended gate system are shown in Table 1.

Table 1. The main electrical parameters of the oscillator and the MOS capacitor dimensions

f_{res}	16 MHz
Q	641
Amplitude	90 mV
Bias current	1 µA
C_2	200 nF
W	6 µm
L	34 µm
t_{ox}	40 nm
air gap	300 nm

Comparing to oscillators based on integrated components, they present a bigger quality factor [9] $Q \in (1\ 000,\ 500\ 000)$, but much lower than quartz. Because the change of the capacitance with the bias voltage, and the dependence of the resonating frequency on those capacitance, frequency can be slightly varied.

Another disadvantage is the large motional resistance that is important for the maintenance of the oscillations. This can be resolved in two ways. First the gap should be smaller or, the second way is to use an array of the same device. In the better case, the matching of frequency can be a huge problem [10].

8. Conclusions

The work presented the suspended gate MOS (SG-FET) in the vibrating-mode regime. The small signal equivalent circuit was developed and validated by simulation. Based on this scheme an oscillator was conceived and simulated. The results were validated by matching the results with a real transistor that had the same dimensions and was made out of the same materials.

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