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High Density and Low Leakage Current Based 5T SRAM Cell Using 45 nm Technology

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Abstract. This paper is based on the observation of a CMOS five-transistor SRAM cell (5T SRAM cell) for very high density and low power applications. This cell retains its data with leakage current and positive feedback without refresh cycle. This 5T SRAM cell uses one word-line and one bit-line and extra read-line control. The new cell size is 21.66% smaller than a conventional six-transistor SRAM cell using same design rules with no performance degradation. Simulation and analytical results show purposed cell has correct operation during read/write and also the delay of new cell is 70.15% smaller than a six-transistor SRAM cell. The new 5T SRAM cell contains 72.10% less leakage current with respect to the 6T SRAM memory cell using cadence 45 nm technology.

Key words: 5T SRAM Cell, Cell delay, Cell leakage, Cell area, Power consumption.

1. Introduction

Fast low power SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the on-chip memory cell sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory. The power dissipation has become an important

consideration due to the increased integration, operating speeds and the explosive growth of battery operated appliances. The leakage current of the memory will be increased with the capacity such that more power will be consumed even in the standby mode. These on-chip memory cells are usually implemented using arrays of densely packed SRAM cells for high performance [1]. A six transistor SRAM cell (6T SRAM cell) is conventionally used as the memory cell [2]. However, the 6T SRAM cell produces a cell size an order of magnitude larger than that of a DRAM cell, which results in a low memory density [2]. Therefore, conventional SRAMs that use the 6T SRAM cell have difficulty meeting the growing demand for a larger memory capacity in mobile applications [2].

Studies show that the power dissipated by the cell is usually a significant part of the total chip power [1]. Cell accesses consume a significant fraction (30-60%) of total power dissipation in modern microprocessor [3]. A large portion of cell energy is dissipated in driving the bit-lines, which are heavily loaded with multiple storage cells [3]. Clearly, the memory cells are the most attractive targets for power reduction [1]. Besides, in cell accesses an overwhelming majority of the write and read bits are '0'. Whereas in the conventional SRAM cell because one of two bit-lines must be discharged to low regardless of written value, the power consumption in both writing '0' and '1' are the generally same [1]. Also in conventional SRAM cell differential read bit-line used during read operation and consequently, one of the two bit-lines must be discharged regardless of the stored data value [3]. Therefore always there are transitions on bit lines in both writing '0' and reading '0' and since in cell accesses an overwhelming majority of the write and read bits are "0" these cause high dynamic power consumption during read/write operation in conventional SRAM cell.

The read static noise margin (SNM) is important parameter of SRAM cell. The read SNM of cell shows the stability of cell during read operation and further degraded by supply voltage scaling and transistor mismatch. The read operations at the low read SNM levels result in storage data destruction in SRAM cells [4].

In response to these challenges in conventional SRAM cell, our objective is to develop a read-static-noise margin- free SRAM cell with five transistors to reduce the cell area size with performance and power consumption improvement. In designing of this new cell we exploit the strong bias towards zero at the bit level exhibited by the memory value stream of ordinary programs.

2. Read static noise margin and SRAM cell current in conventional SRAM cells

The SRAM cell current and read static noise margin (SNM) are two important parameters of SRAM cell. The read SNM of cell shows the stability of cell during read operation and SRAM cell current determine the delay time of SRAM cell [4]. Fig.1 shows the SRAM cell current in the conventional SRAM cell. Although SRAM cell current degradation simply increases bit-line (BL) delay time, Read SNM degradation results in data destruction during Read operations [4]. Both Read SNM and SRAM cell current values are highly dependent on the driving capability of the access NMOS

transistor: Read SNM decreases with increases in driving capability, while SRAM cell current increases [4]. That is, the dependence of the two is in an inverse correlation [4]. Thus in conventional SRAM cell the read SNM of cell and cell current cannot adjust separately.

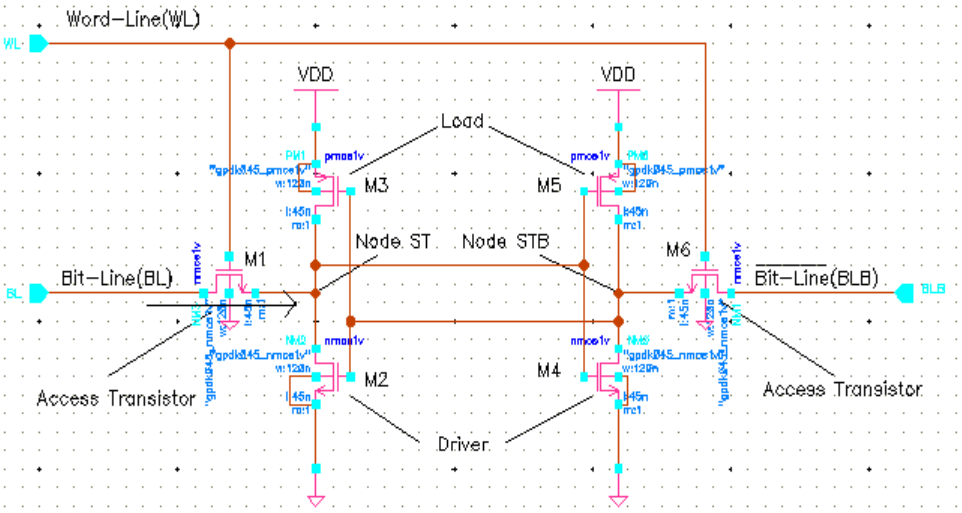

Fig. 1. SRAM cell current in 6T SRAM cell.

One strategy for solving the problem of inverse correlation between SRAM cell current and read SNM is separation of data retention element and data output element. Separation of data retention element and data output element means that there will be no correlation between Read SNM and SRAM cell current. Base on this strategy, [5] presents a dual-port SRAM cell. But this cell is composed of eight transistors and has 30% greater area than that of a conventional 6T SRAM cell [4]. Another strategy is loop-cutting during read operation. Base on this strategy in [4] a read-static-noise-margin-free SRAM cell for low-VDD and high speed application presented. To avoid inverse correlation between SRAM cell current and read SNM we proposed new five transistor SRAM cell. Our proposed cell is base on loop-cutting strategy and this observation that in ordinary programs most of the bits in memory cell are zeroes for both the data and instruction streams. This new cell making it possible to achieves both low-VDD and high-speed operations with no area overhead.

3. Cell design concept

Figure 2 shows a circuit equivalent to a developed 5T SRAM cell using a supply voltage of 1.1V in 45-nm technology node. During idle mode of cell (when read and write operation don't perform on cell) the feedback cutting transistor (M5) is ON and N node pulled to VDD by this transistor. When '1' stored in cell, M3 and M2 are ON and there is positive feedback between ST node and STB node, therefore ST node

pulled to VDD by M2 and STB node pulled to GND by M3. When '0' stored in cell M4 is ON and since N node maintained at VDD by M5 the STB pulled to VDD, also M2 and M3 are OFF and for data retention without refresh cycle following condition must be satisfied.

$$I_{DS-M1} > I_{SD-M2} + I_{gate-M4} + I_{gate-M3} \tag{1}$$

For satisfying above condition when '0' stored in cell, we use leakage current of access transistors (M1), especially sub-threshold current of access transistors (M1).

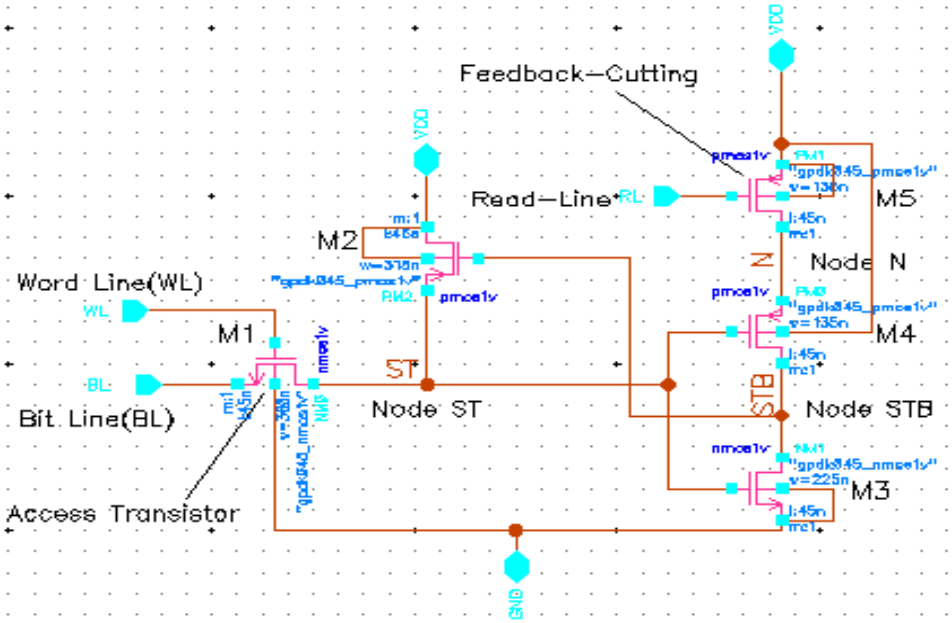

Fig. 2. New 5T SRAM cell in 45-nm technology node.

For this purpose during idle mode of cell, bit-line maintained at GND and word-line maintained at VIdle. Figure 3 shows leakage current of cell during idle mode for data retention when '0' stored in cell. Most of leakage current of access transistor (M1) is sub-threshold current, since this transistor maintained in sub-threshold region.

Cadence Virtuoso simulation result with VDD = 1.1 V shows if during idle mode of cell, bit-line maintained at GND and VIdle = 0.2 V then '0'data stored in cell without refresh cycle and thus in idle mode above condition satisfied. The Cadence Virtuoso parameters are obtained from the latest for the technology node of 45-nm [6].

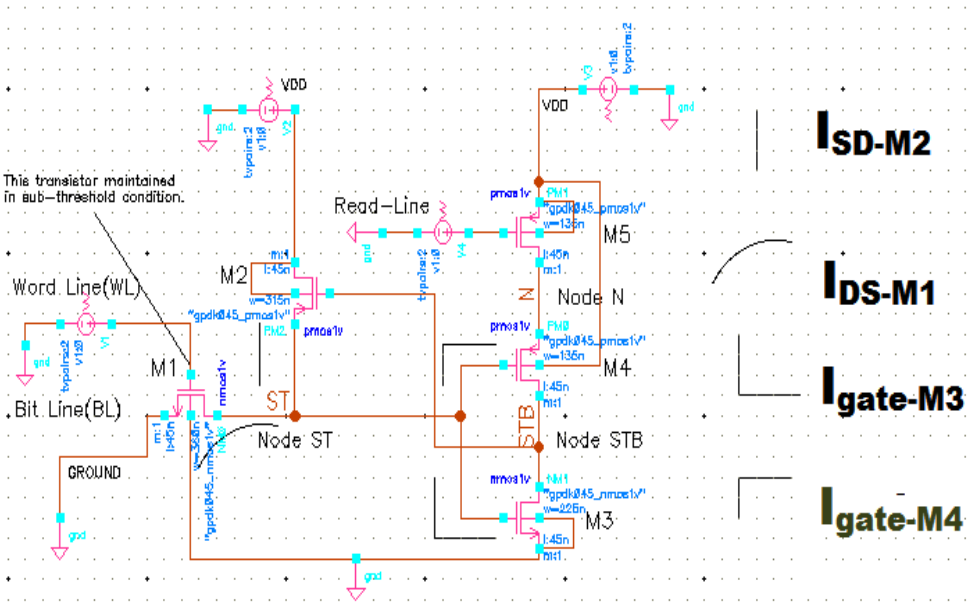

Fig. 3. Leakage current in idle mode when '0' stored in cell.

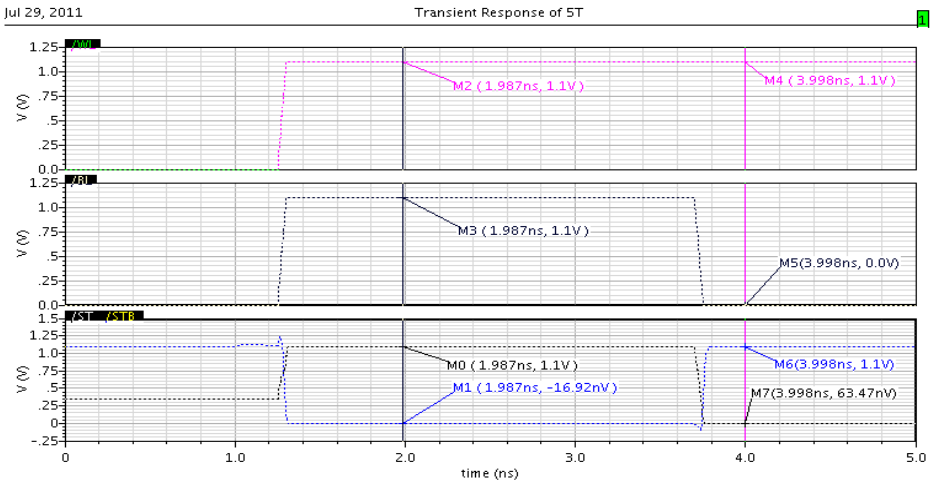

Fig. 4. Waveform of new cell during write cycle.

4. Read and write operation

During write operation feedback-cutting transistor is ON and N node pulled to VDD by this transistor, thus in write operation read-line maintained at GND. When a write operation is issued the memory cell will go through the following steps.

1. Bit-line driving: For a write, data drove on bit-line (BL), and then word-line (WL) asserted to VDD.
2. Cell flipping: this step includes two states as follows:
   a) Data is zero: in this state, ST node pulled down to GND by NMOS access transistor (M1), and therefore the Load transistor (M4) will be ON, and STB node will be pulled up to VDD.
   b) Data is one: in this state, ST node pulled up to VDD-VTN by NMOS access transistor (M1), and therefore the drive transistor (M3) will be ON, and STB node will be pulled down to GND, thus load transistor (M2) will be ON and positive feedback created by M2 and M3.
3. Idle mode: At the end of write operation, cell will go to idle mode and word-line and bit-line asserted to VIdle and GND, respectively.

When a read operation is issued the memory cell will go through the following steps.

1. Bit-line discharging: For a read, bit-line discharged to GND, and then floated. Transistor is OFF and thus read-line maintained at VDD during read operation.
2. Word-line activation: in this step word-line asserted to VDD and two states can be considered:
   a) Voltage of ST node is high: when voltage of ST node is high, the voltage of bit-line pulled up to high voltage by NMOS access transistor. We refer to this voltage of bit-line as VBL-High.
   b) Voltage of ST node is low: when voltage of ST node is low, the voltage of bit-line and ST node equalized.
3. Sensing: After word-line deactivate to VIdle and read line return to GND then sense amplifier is turned on to read data on bit-line. Figure 5 shows possible circuit schematic of sense amplifier that used for reading data from new cell.
4. Idle mode: At the end of read operation, cell will go to idle mode and bit-line asserted to GND, respectively.

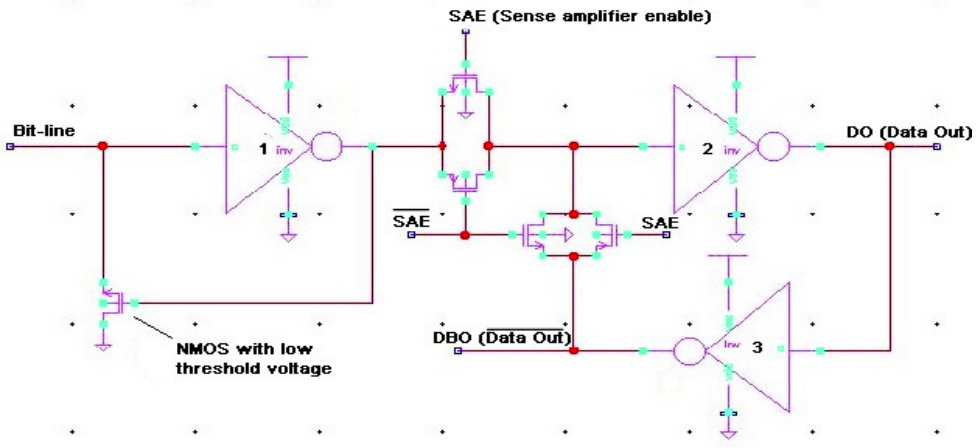

Fig. 5. Possible circuit schematic of sense amplifier.

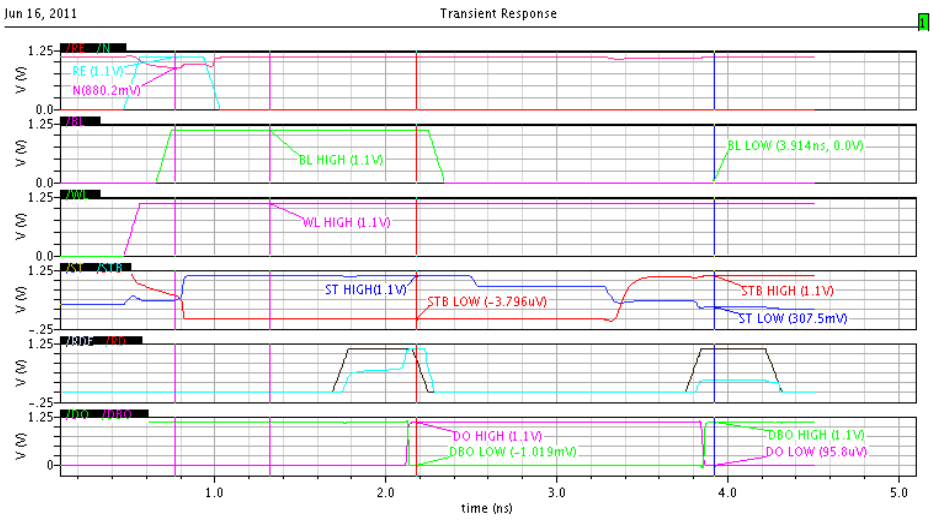

Fig. 6. Waveform of new cell during read cycle.

5. Cell area

Figure 7 shows the layout of 6T SRAM cell and Fig. 8 shows the 5T SRAM cell in scalable CMOS design rules. The 6T SRAM cell has the conventional layout topology and is as compact as possible. The 6T SRAM cell requires 3.438 μm^2 areas, whereas 5T SRAM cell requires 2.69 μm^2 areas.

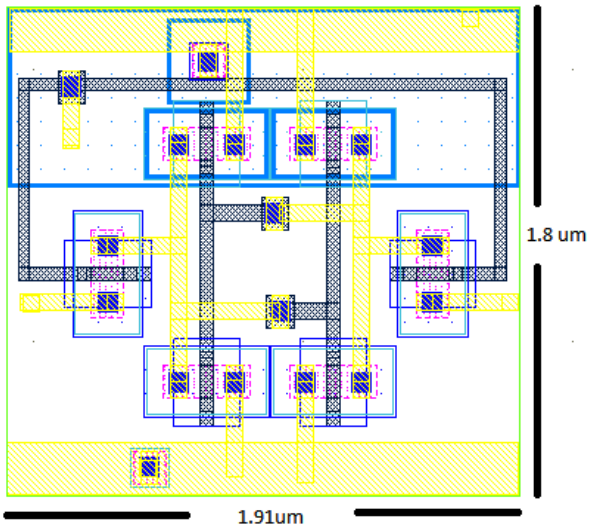

Fig. 7. Layout of 6T cell using 45 nm technology.

These numbers do not take into account the potential area reduction obtained by sharing with neighboring cells. Therefore the new cell size is 21.66% smaller than a conventional six-transistor cell using same design rules

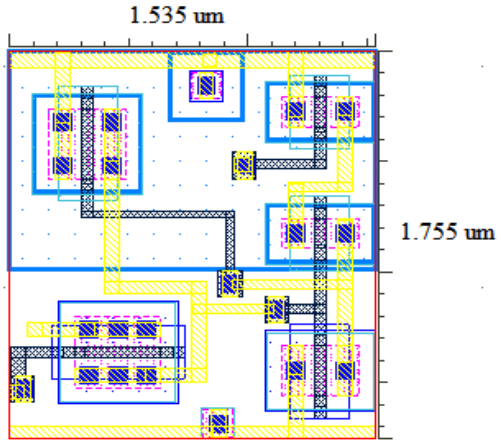

Fig. 8. Layout of 5T cell using 45 nm technology.

6. Leakage current

In one state, novel 5T SRAM cell must retains its data using the leakage current of the access transistor (when zero stored) and in the other state the 5T SRAM cell must retains its data using positive feedback (when one stored). Thus in idle mode when '1' stored in cell, there is positive feedback and M2, M3 and feedback cutting (M5) transistors are ON and access transistor maintained in sub-threshold region. In this state there is a path from supply voltage to ground and power dissipated.

Leakage current will be calculated from the equation below at the time when transistor is in off condition [14].

$$I_{sub} = \mu_0 c_{ox} \frac{W}{L_{eff}} V_T^2 e^{1.8} \exp\left(\frac{V_{gs} - V_{th}}{nV_T}\right) \cdot \left(1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right) \tag{2}$$

Figure 8 shows this path when '1' stored in cell. In ordinary programs most of the bits in memory cell are zeroes for both the data and instruction streams. It has been shown that this behavior persists for a variety of programs under different assumptions about memory cell sizes, organization and instruction set architectures [7] [8]. Thus most of bit values resident in the data and instruction memory cell are zero. Based on these observations we simulated average leakage current in idle mode of 5T SRAM cell and conventional 6T SRAM cell by using 45 nm technology.

6.1. Diffusion Leakage

Although diffusion leakage ($I_{diffusion}$) did not pose a significant technical challenge for the ULP technology leakage goals, some experimental optimization was

required to reach them. Reverse-Bias Diffusion Leakage (RBDL) is a function of defect population within the depletion region and the local stresses arising from sources such as STI (Shallow Trench Isolation) processing parameters and silicide processing [13]. This leakage can be characterized as:

$$I_{diffusion} = A_2 \exp\left(E_a / K_T\right), \tag{3}$$

where E_a is roughly equal to E_g / 2 in the typical junction environment, and A_2 is defined as:

$$A_2 = T^{3/2} \times V^{1/2}. \tag{4}$$

The diffusion leakage was minimized by optimizing the source/drain energy, so that the junction depth was deep enough to avoid silicide defects. The relationship between the deep p-well retrograde implant and area diffusion leakage resulted in a reduction of the deep retrograde implant dose for the ULP technology.

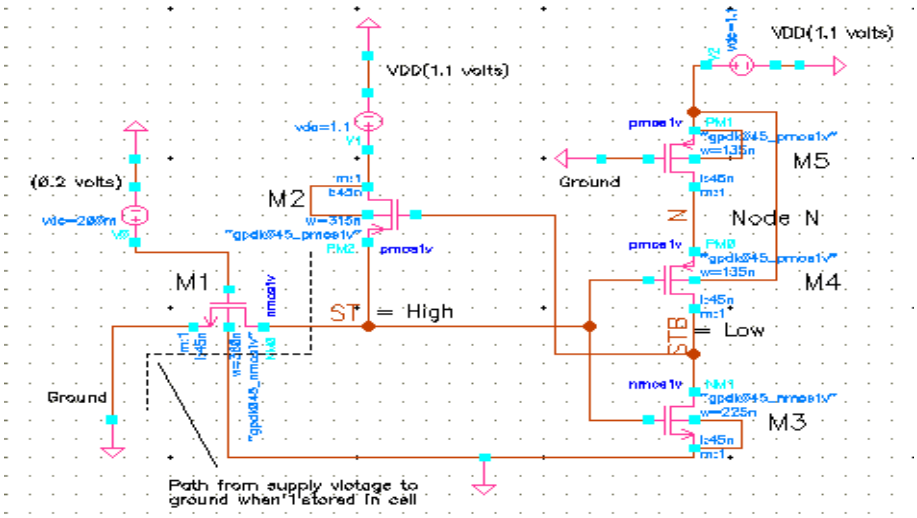

Fig. 9. Path from supply voltage to ground.

6.2. Process of calculating leakage current

Leakage current is calculated from that transistor which is in off condition at the time of operation. In the leakage current calculation there are four operations performed and it is described below.

a) For write1 in STB node

For writing 1 in STB node, transistor M3 will be in OFF condition so we will take leakage current from the node of M3 transistor.

Leakage current at STB node for writing 1 = leakage at M3 transistor = –9.824 nA.

b) For write0 in STB node

For writing 0 in STB node, transistor M4 will be in OFF condition so we will take leakage current from the node of M4 transistor.

Leakage current at STB node for writing 1 = leakage at M3 transistor = 5.51 nA.

c) For write 1 in ST node

For writing 1 in ST node, transistor M4 will be in OFF condition so we will take leakage current from the node of M4 transistor.

Leakage current at STB node for writing 1 = leakage at M3 transistor = 18.9 nA.

d) For write 0 in ST node

For writing 0 in ST node, transistor M2 will be in OFF condition so we will take leakage current from the node of M2 transistor.

Leakage current at ST node for writing 0 = leakage at M3 transistor = 3.60 nA.

6.3. Comparison of 5T & 6T for leakage current

Table 1 shows the 5T SRAM cell leakage in write 0 STB node, write 1 ST node, write 0 ST node is less than the 6T SRAM cell. It shows that 5T is better than 6T for write data in SRAM cell.

Table 1. Comparison between 5T & 6T leakage current

No.	Parameters	Leakage current in 5T		Leakage current in 6T		Better Performance
		At 25°C	At 35°C	At 25°C	At 35°C	
1	For write1 in STB node	–9.824 nA	–19.648 nA	–0.229 nA	–0.458 nA	6T
2	For write0 in STB node	5.51 nA	11.02 nA	94.11 nA	188.22 nA	5T
3	For write1 in ST node	18.9 nA	37.8 nA	–32.10 nA	–64.2 nA	5T
4	For write0 in ST node	3.60 nA	7.2 nA	9.20 nA	18.4 nA	5T

7. Cell delay

The propagation delay [12] times τ_{PHL} and τ_{PLH} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively. By definition, τ_{PHL} is the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$ transition of the falling output voltage. Similarly, τ_{PLH} is defined as the time delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\%}$ transition of the rising output voltage. To simplify the analysis and the derivation of delay expressions, the input voltage waveform is usually assumed to be an ideal step pulse with zero rise and fall times. Under this assumption, τ_{PHL} becomes the time required for the output voltage to fall from V_{OH} to the V_{150s} level,

and τ_{PLH} becomes the time required for the output voltage to rise from V_{OL} to the $V_{50\%}$ level. The voltage point $V_{50\%}$ is defined as follows.

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OH} + V_{OL}) \tag{5}$$

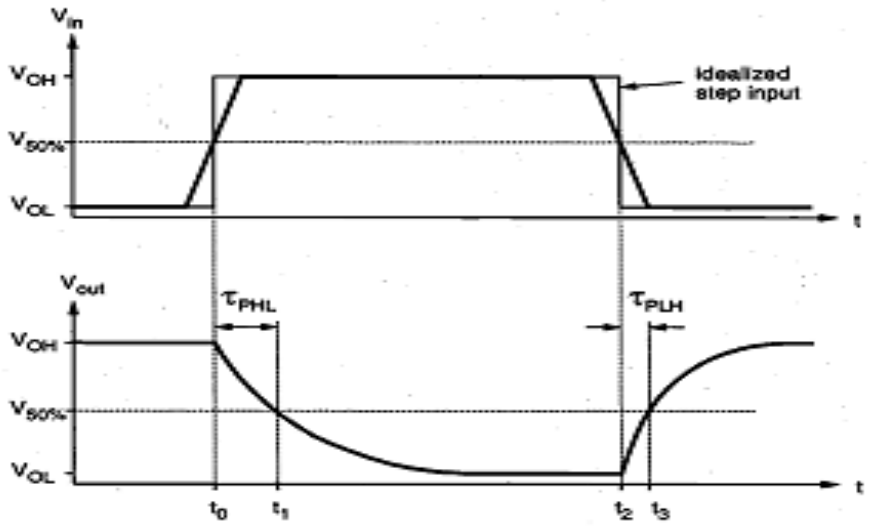

Fig. 10. Input and output voltage waveforms of a typical inverter, and the definitions of propagation delay times. The input voltage waveform is idealized as a step pulse for simplicity.

Thus, the propagation delay times τ_{PHL} and τ_{PLH} are found:
$\tau_{PHL} = t_1 - t_0$, $\tau_{PLH} = t_3 - t_2$.

The average propagation delay τ_p of the inverter characterizes the average time required for the input signal to propagate through the inverter.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}. \tag{6}$$

Cell delay will be calculated directly by using the cadence virtuoso tools. By using the calculator after the simulation of the circuit like 5T SRAM cell, we can calculate the delay in both the condition for ST node and for STB node. The delay will be calculated [11] by using the basic idea which is shown in Fig. 10.

Delay of the cell depends on the consumption of time between the cells from input (BL) to output [10]. Comparison of the cell delay between 5T & 6T shows in Table 2.

Table 2. Comparison between 5T & 6T cell delay

No.	Parameters	Delay of 5T	Delay of 6T	Better Performance
1	Delay at STB	14.24 ps	47.72 ps	5T
2	Delay at ST	2.453 ns	0.839 ns	6T

This table shows that 5T cell delay in STB node is less than 6T cell delay in STB node. It means 5T is better than 6T because the output is taken from the STB node and cell delay for the 5T in STB node is less than the 6T in STB node. Information of comparison between 5T and 6T SRAM cell delay graphically shown in Fig. 11.

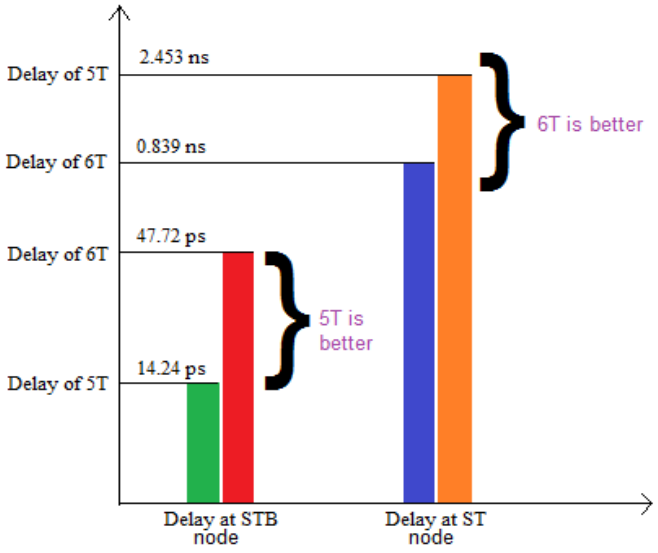

Fig. 11. Delay Comparison between 5T and 6T.

8. Power consumption

Power consumption of the SRAM memory cell is depending on the consumption of the power of the transistor using for the operation [9].

Assuming periodic input and output waveforms, the average power dissipated by any device over one period can be found as follows [12]:

$$P_{av} = \left[(1/T) \int_0^T I \mathrm{d}t \right] \times V \tag{7}$$

By using these phenomena we can calculate power consumption during four operations for 5T SRAM cell.

a) Power consumed at STB node for writing 1

For writing 1 in STB, M1-M4-M5 transistors are on and these transistors are consuming power and which is calculated by multiplying voltage and current of that transistors.

$$P_{consumed-STB-writing\,1} = P_{M1} + P_{M4} + P_{M5} = 9.8\,\mathrm{nW}$$

b) Power consumed at STB node for writing 0

For writing 0 in STB, M1-M3 transistors are on and these transistors are consuming power and which is calculated by multiplying voltage and current of those transistors.

$$P_{consumed-STB-writing\,1} = P_{M1} + P_{M3} = 67.3\,\text{nW}$$

c) Power consumed at ST node for writing 1

For writing 0 in STB, M2-M3 transistors are on and these transistors are consuming power and which is calculated by multiplying voltage and current of those transistors.

$$P_{consumed-STB-writing\,1} = P_{M2} + P_{M3} = 85.01\,\text{nW}$$

d) Power consumed at ST node for writing 0

For writing 1 in STB, M1-M4-M5 transistors are on and these transistors are consuming power and which is calculated by multiplying voltage and current of those transistors.

$$P_{consumed-STB-writing\,1} = P_{M1} + P_{M4} + P_{M5} = 9.8\,\text{nW}$$

Power consumption of the cell is shows in Table 3.

Table 3. Comparison between 5T & 6T power consumption

No.	Parameters	Power consumption of 5T	Power consumption of 6T
1	Power consumed at STB node for writing 1	9.8 nW	0.011 pW
2	Power consumed at STB node for writing 0	67.3 nW	30 pW
3	Power consumed at ST node for writing 1	85.01 nW	0.003 pW
4	Power consumed at ST node for writing 0	9.8 nW	28 pW

9. Conclusion

With the aim of achieving a high density and low leakage current memory cell, we developed a 5T SRAM cell. The key observations behind our design are that the cell leakage is determined from that node in which the transistor is off. In same design rules proposed cell area is 21.66% smaller than 6T SRAM cell with 28.57% speed improvement. Leakage current during memory cell access of new cell is 72.10% lesser than 6T SRAM cell and every 10 $^\circ$ C temperature increment leakage current doubles to its values but the proposed cell is cell power consumption penalty.

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