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High Temperature Compensated Voltage Reference Integrated Circuits on 4H-SiC Material

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Abstract. This work demonstrates a functional fabricated high temperature compensated Voltage Reference (VR) integrated circuit on 4H-SiC material. The study starts with an experimental analysis on the feasibility on silicon carbide (SiC) of the widely used bandgap reference concept both with Schottky and bipolar diodes. Then an original solution is proposed for a special finger type MESFET. Our approach of the MESFET design overcomes the typical embedded drain leakage of finger type MESFET. This device design was specially developed for using in analog schematics on SiC. Further, an original VR schematic is proposed avoiding the bandgap reference topology and accordingly avoiding an operational amplifier (OpAmp), which is not yet developed on SiC. The performed measurements on the fabricated integrated circuits show a temperature coefficient (TC) comparable to the normal bandgap voltage references on silicon but this SiC circuit is able to work up to 300°C, compared to 125°C for silicon or 200°C for SOI (silicon on insulator). A very important progress of our work is the integration of the presented circuit on the same SiC chip with a power lateral MESFET. Additionally, the circuit contains a linear temperature sensor useful for over temperature protection.

Key-words: integrated circuit, bandgap reference, silicon carbide, SiC, voltage reference, high temperature, thermal compensated, power, MESFET.

1. Introduction

The market of discrete power Silicon Carbide devices has a continuous developing; a large variety of SiC devices is now available from various suppliers. However, for the control circuitry on SiC able to work in harsh environment, there is still little progress. The mostly reported are the SiC digital integrated circuits [1–8]. Very few reports exist on the topic of analog Integrated Circuits (IC) built on silicon carbide (SiC) [9–12].

Providing internal high precision voltage reference insensitive to temperature is a very important function for the analog and mixed-signal integrated circuits.

We have previously demonstrated the feasibility of SiC bandgap voltage reference that is possible to be implemented both with Schottky and bipolar diodes or bipolar transistors [13, 14]. The main issue of SiC bandgap reference is the lack of ICs developed on SiC that does not permit to integrate on the same chip such a reference topology. Therefore we developed a new approach in order to obtain an integrated voltage reference on SiC, able to operate up to 250°C and even beyond.

Planar technology and scalability of transistors are crucial aspects for a successful integrated circuit on SiC. Since the MOSFET on SiC technology is still immature, we have developed a SiC MESFET technology that is planar and scalable, in order to produce integrated circuits [1, 2, and 15]. This technology is based on MESFET devices with tungsten gates [16], epitaxial resistors, P-implanted isolated tubs and three metallization levels.

The SiC voltage reference as essential analog building block circuit is intended to bring a contribution to the development of the further analog IC on SiC material.

2. Bandgap voltage reference

2.1. Theory of operation

2.1.1. Basic Equations

It is commonly stated for silicon analog circuits, that the bandgap voltage reference value depends on the band gap of the semiconductor [17, 18]. This dependence comes from the use of Si bipolar conduction devices, whose saturation current I_{Sat} depends on the intrinsic concentration and consequently on the band gap [19–21]. In fact, any voltage signal pair exhibiting complementary temperature dependence can be used to obtain a stable voltage reference, simply compensating each other. The key of any bandgap reference is the presence of devices with an exponential $I - V$ characteristic, such as diodes (bipolar or Schottky) or bipolar transistors (Eqs. 1–2). At low current densities, the voltage drop due to series resistances is negligible and the diode, and particularly the SiC Schottky diode, behaves predictable electrical and thermal characteristics, described by analytical equations (Eqs. 1–3): I_D, I_{Sat} and V_D are the forward current, the saturation current and the voltage drop across the Schottky diode, respectively. T, q, k and n, are the absolute temperature, the electron charge, the Boltzmann's constant and the ideality factor, respectively.

2.1.2. Principles of the thermal compensation

If a constant current flows through the Schottky diode in the forward conduction mode, the voltage drop V_D exhibits a slight parabolic negative temperature coefficient (Fig. 1a). As inferred from Fig. 1, the voltage difference between two diodes biased at different current densities increases with temperature (increases the distance between the two curves). This voltage difference is also plotted in (Fig. 1a). The chosen ratio of the two diode's currents is $M = 20$.

$$I_D = I_{Sat}\left(e^{\frac{qV_D}{nkT}} - 1\right) \tag{1}$$

For $V_D > 3kT/q$, the exponential factor $e^{\frac{qV_D}{nkT}} \gg 1$, so eq. (4) simplifies to

$$I_D = I_{Sat} \cdot e^{\frac{qV_D}{nkT}} \tag{2}$$

$$V_D = \frac{nkT}{q} \ln \frac{I_D}{I_{Sat}} \tag{3}$$

$$\Delta V_D = V_{D2} - V_{D1} = \frac{nkT}{q} \ln \frac{I_{D2}}{I_{D1}} = \frac{nkT}{q} \ln M = V_{PTAT} \tag{4}$$

where $M = \dfrac{I_{D2}}{I_{D1}}$ is the diode's current ratio.

The difference voltage between D1 and D2 called V_{PTAT} (proportional to absolute temperature) exhibit a fully linear positive temperature coefficient (Eq. 4). Having the two temperature dependent voltages V_{D2} and V_{PTAT} with opposite sign of the TC, we can combine these signals in order to obtain a temperature compensated voltage reference (VR). The reference voltage is given by (Eq. 5):

$$V_{BG} = V_{D2} + KV_{PTAT}, \tag{5}$$

V_{PTAT} is amplified by a factor K in order to produce the same absolute value of the TC for the two signals in a given temperature point (Fig. 1b).

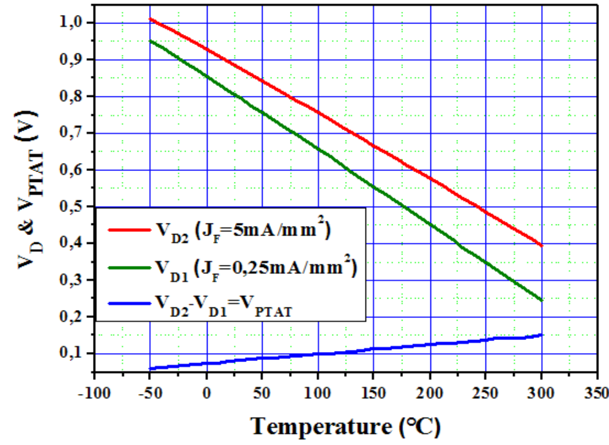


Fig. 1a.

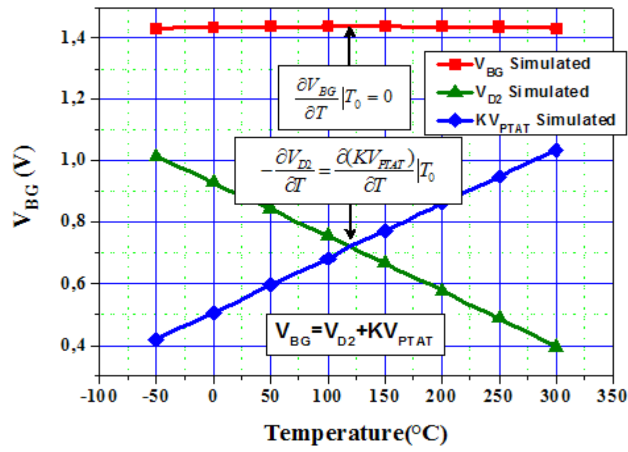


Fig. 1b.

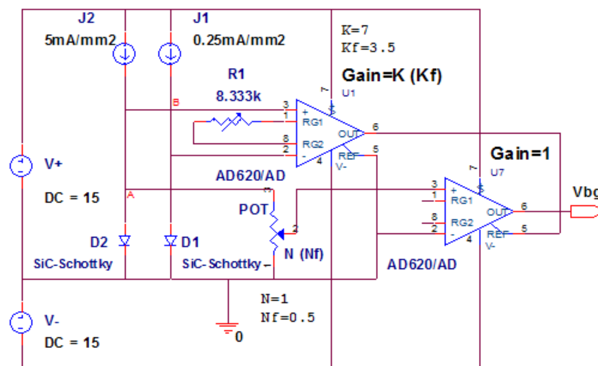


Fig. 1c.

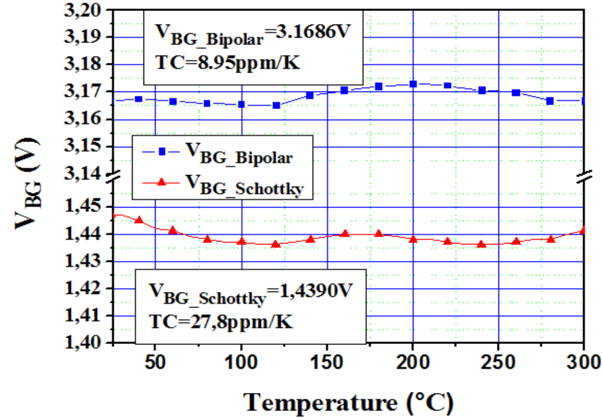


Fig. 1d.

Fig. 1. (a) Voltage drop across the diodes D1, D2 and the resulting V_{PTAT}; **(b)** approaching the bandgap reference voltage as a sum of two voltages with opposite TC; **(c)** principle schematic of the test circuit for the SiC bandgap VR; **(d)** Experimental results of bandgap VR obtained by using both Schottky and bipolar SiC diodes.

The examples illustrated in Fig. 1a and Fig. 1b is calculated using SiC Schottky diodes. Figure 1c shows the schematic of the test circuit used for the SiC bandgap reference with both Schottky and bipolar diodes. Figure 1d presents the voltage output of the experimental SiC bandgap voltage reference for the implementation with bipolar and Schottky SiC diodes.

The aim of this demonstration is to find the voltage reference values that we can expect from the bandgap architecture applied on SiC material. The demonstration showed that the principle of the bandgap architecture is valid also on SiC. In the case of bipolar diodes, the output voltage reference is roughly V_{BGbip}=3.17 V , close to the 4HSiC bandgap E_G=3.26 eV. A similar result we can expect using bipolar SiC transistors instead of bipolar diodes. In this case, the ideality factor $n = 1$.

Note that in this demonstration, the operational amplifier (OP-Amp) is external, and it was not exposed to the high temperature. The work is useful for the future development of fully integrated bandgap voltage reference architecture.

3. Integrated Voltage Reference Circuit with MESFETs

3.1. Planar Finger Type MESFET Design

The first essential step in order to obtain an analog circuit was the development of a finger type gate MESFET capable of low leakage off state. The finger gate MESFETs ensures easily the concept of transistor multiplicity. Another important requirement for the transistors and resistors in the schematic is the use of a planar technology that minimizes the metal interconnections steep steps of the schematic layout. Therefore, implanted isolation walls were used instead of the standard close

loop gate with etched isolation. This technology ensured the obtaining of scalable and planar devices.

Anyway, a minimum distance between the P isolation wall and the gate edge would remain with the associated residual leak channels [12]. In order to overcome this drawback, a metal-oxide overlap was deposited onto the leakage channels aiming to transform this leakage channel into an oxide-gate residual MESFET. The oxide gate residual MESFET is able to completely deplete the residual channel at higher pinch off voltage than the main MESFET (Fig. 1), thus resulting a double pinch off voltage, one for the main MESFET and the second for the parasitic oxide gated MESFET.

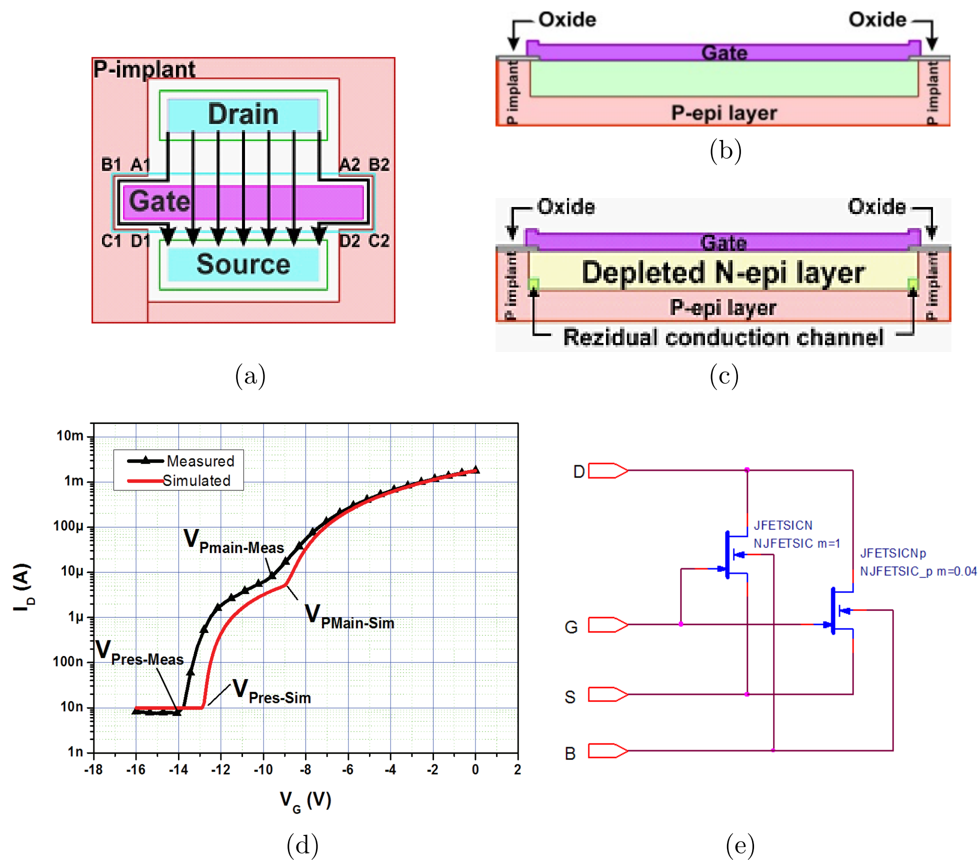


Fig. 2. (a) Basic finger gate MESFET layout and current flow distribution, (b) cross section through the non depleted gate, (c) cross section through depleted gate of the main transistor and residual channel @ $V_{GS} = V_{pinch-off}$, V_{DS}=0, (d) $I_D - V_D$ characteristics of planar finger gate MESFET, (e) electrical equivalent circuit of the composed MESFET.

3.2. Design Schematic

3.2.1. Comment on reference generators

The widely used voltage references are Zener diodes, Bandgap references, XFET Reference (Analog Devices^{TM}) and recently, the Xicor Floating Gate Analog Voltage Reference. Excepting Zener diodes, the architecture of the other types of voltage reference is based on the signal processing with operational amplifiers and current mirrors. The lack of the silicon carbide operational amplifiers (OpAmp) forecloses actually the development of bandgap voltage reference on SiC.

3.2.2. Design description

Specific to the bandgap voltage reference is combining the PTAT signal (**P**roportional **T**o **A**bsolute **T**emperature with CTAT signal (**C**omplementary **T**o **A**bsolute **T**emperature), where the PTAT is generated by the voltage difference of two diodes or bipolar transistor. To avoid the lack of SiC OpAmp inconvenience, a new architecture has been developed. In our new approach, quadratic signals versus temperature having complementary behavior are used for suppressing the temperature dependence.

The schematic design is presented in Fig. 3. It comprises three modules having different functions. The first module is a voltage regulator that generates a relatively constant output voltage supply V_{O1} for the others modules. This module, called Pre-regulator, performs two other additional functions: partial thermal compensation and improving the Power Supply Rejection Ratio (PSRR) of the voltage reference.

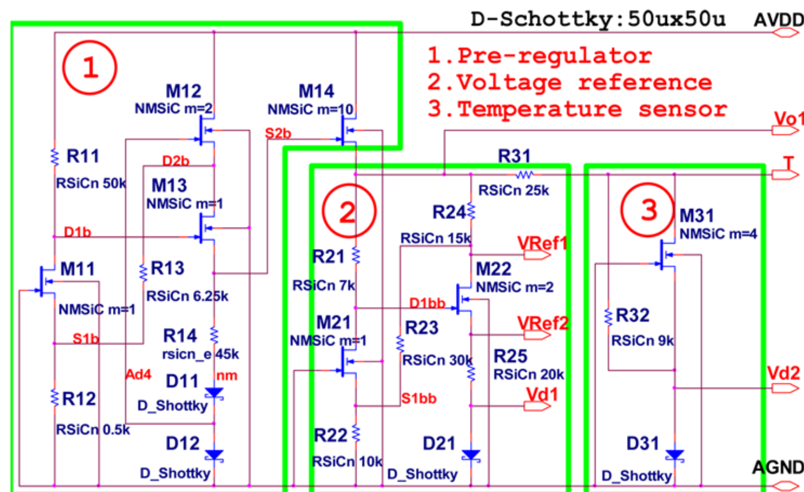


Fig. 3. Schematic of the voltage reference IC on SiC and micrograph of the SiC Voltage reference.

The second module, Voltage reference, provides the thermally compensated voltage with low temperature coefficient TC. The transistors M21 and M22 generate a

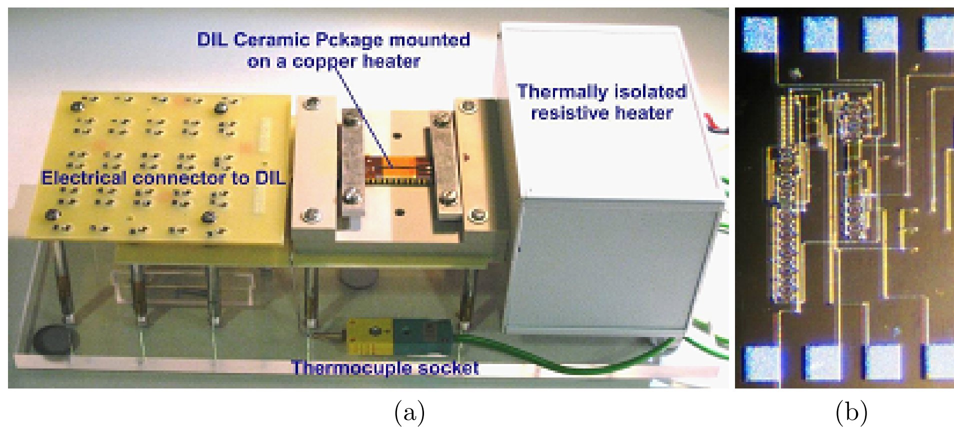
constant current that is applied to the Schottky diode D21. The negative TC voltage drop on the Schottky diode D21 is compensated by the SiC resistor R25 and the MESFET M22. The resistor R23 provides a negative feedback that maintains constant the current through the Schottky diode D21. The third module, temperature sensor, generates a linear CTAT signal (complementary to absolute temperature). The resistors R31, R32 and the MESFET M31, compensate the parabolic TC of the Schottky diode D31 thus obtaining a linear temperature dependence. The temperature sensor is useful for temperature measurement and for over-temperature protection.

3.2.3. Design Simulation and Layout

For simulation, a SPICE model library was elaborated, using extracted parameters from experimental measurements performed on finger gate planar MESFETs, n-epitaxial resistors and Schottky diodes. The design was simulated and optimized using these models [1, 2].

3.2.4. Experimental Results

We performed the measurements on 40 DIL ceramic encapsulated devices. We have used a home designed temperature setup (Fig. 4a) up to 250°C. The digital voltmeter model 2400 and the data acquisition software are provided from Keithley.



(a) (b)

Fig. 4. **(a)** Setup of temperature measurement up to 250°C for DIL40 ceramic packaged devices; **(b)** microscope capture of the packaged voltage reference.

Figure 4b shows a micrograph of the fabricated voltage reference circuit.

Compared to the simulation, there is a drift of the experimental output level of the voltage references. The voltage level of V_{O1} and V_{Ref1} are smaller than designed. A possible reason is the parameter's dispersion of fabricated devices, relative to the SPICE model, normally due to the technological dispersions. However, the circuit preserves its functionality. The reference voltage level could be further corrected to the desired value as usual practice of trimming techniques of a supplementary buffer.

The experimental results of the voltage reference are presented in Fig. 5. The measured voltage at the V_{Ref1} output (see the schematic in Fig. 3) for three chips are: $V_{Ref1-1} = 4.9$ V, $V_{Ref1-2} = 5.4$ V, $V_{Ref1-3} = 5.5$ V and achieve in the 25°C–250°C temperature range the temperature coefficients TC1=15 ppm/°C, TC2=33 ppm/°C and TC3= 23 ppm/°C, respectively. For comparison, the temperature dependence of one 6 V silicon Zener diode, with TC=500 ppm/°C is also labeled in Fig. 5.

The TC values of SiC Zener reported in the literature are 57 ppm/°C [22], and in the 80 ppm/°C – 300 ppm/°C range, depending on the breakdown voltage. No temperature range was reported for these diodes. The silicon bandgap voltage references are able to achieve TC values as small as 2–5 ppm/°C [23], using techniques of second order curvature compensation. However, these values are usually obtained for temperatures below 100°C. These comparisons demonstrate that the proposed voltage reference circuit offers much lower temperature drift than Si Zener diodes, and similar values to the Si bandgap references with no curvature compensation, but at a much higher temperature range, up to 300°C.

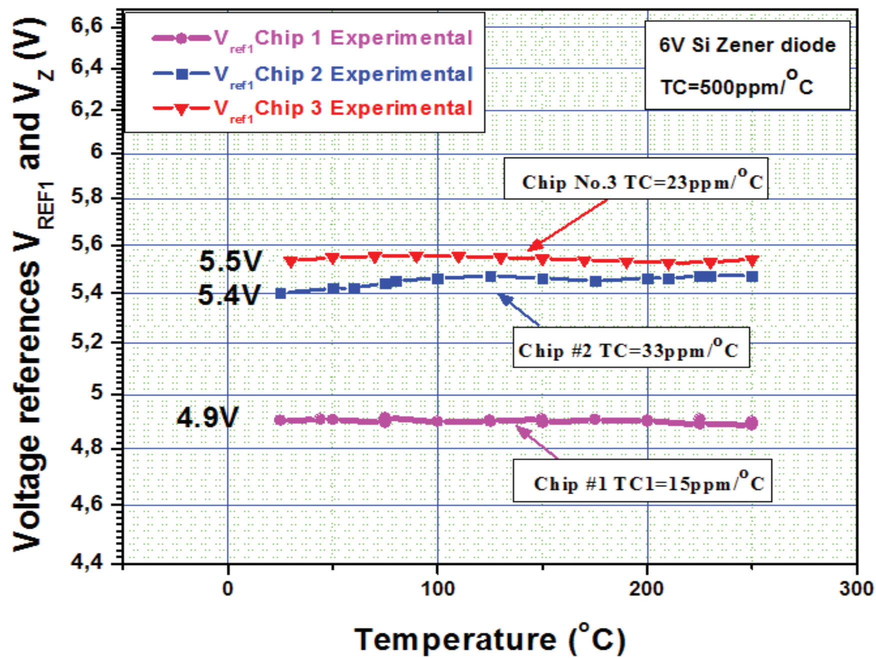


Fig. 5. Experimental voltage reference of three devices; comparison of TC to a low voltage drift Zener diode.

Figure 6 illustrates the experimental Power Supply Rejection Ratio (PSRR) measured by two techniques at room temperature, using both parallel and series sinusoidal ripple signal to the input. Compared to other type of voltage reference, even our schematic achieve a value of only PSRR=–35 dB, in change, the frequency range is many orders of magnitude wider.

This wider frequency range is due to the absence of OpAmp in the schematic architecture. This kind of OpAmp-less architecture avoids the issues of frequency instability as well. The measured frequency rejection bandwidth is in a good agreement with the simulated results. However the rejection ratio shows 20 dB more than the simulation. This is probably due to the parasitic coupling of the PSRR experimental measurements.

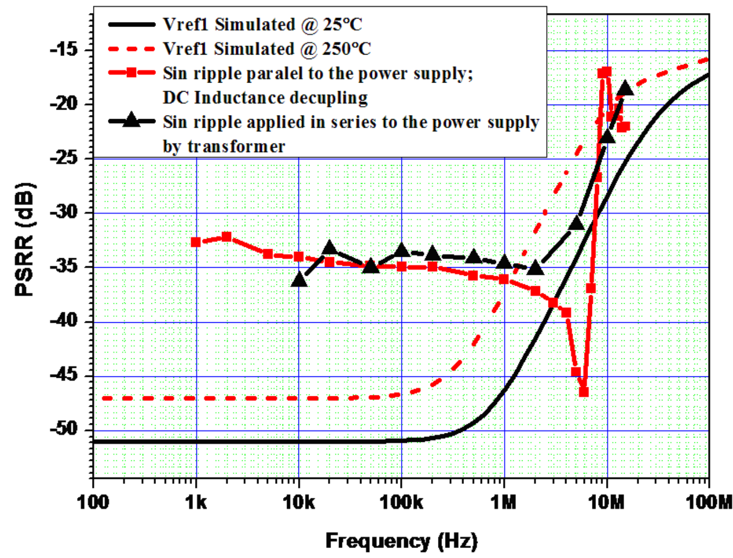


Fig. 6. Simulated and experimental PSRR measured by two measure techniques.

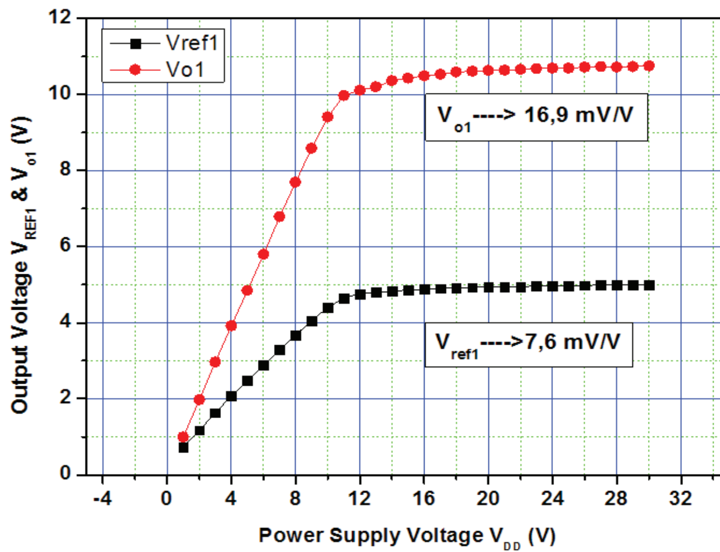


Fig. 7. Experimental power supply regulation at 25°C.

Figure 7 plots the experimental power supply regulation curve of the voltage reference V_{Ref1}, and the pre-regulator V_{O1} at 25°C. The power supply regulation ratio is 7.6 mV/V for the V_{ref1} and 16.9 mV/V for V_{O1} respectively.

The temperature sensor characteristic is illustrated in Fig. 8. The temperature dependence of the sensor has a good linearity, which is described by the correlation factor of the experimental points, $R = -0.99979$, very close to $R = -1.0$ (ideal negative slope line).

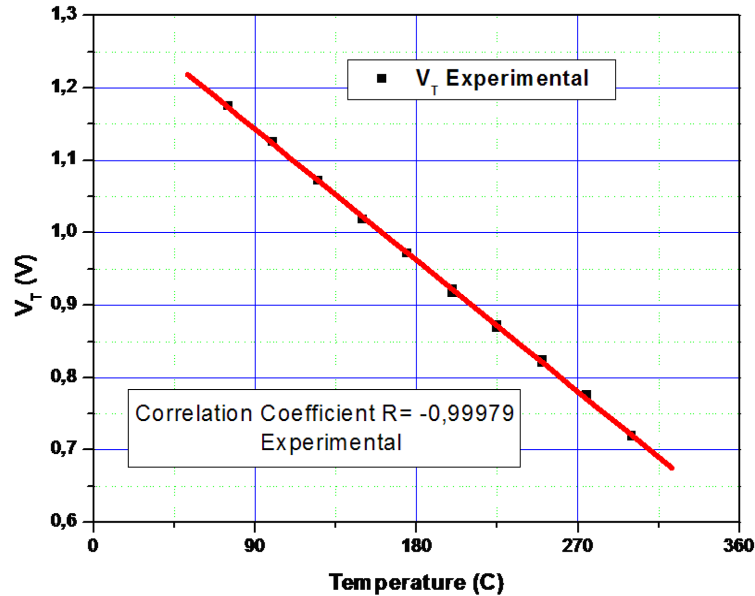


Fig. 8. Temperature sensor characteristic.

The circuit currents consumption for $V_{DD} = 30$ V are 1.8 mA@25°C, 1.35 mA @100°C, 0.82 mA@200°C and 0.55 mA@300°C. As expected, the current decreases with the temperature, due to the SiC resistivity increase.

3.2.5. Simple application demonstration

Figure 9a shows a demonstration with a simple schematic application of the proposed voltage reference. The voltage reference is capable of driving an output power transistor that is either a monolithic integrated SiC MESFET NM1 on the same chip with the VR (Fig. 9b) [9], or an external high voltage HV 3A SiC JFET. The output characteristics are showed in Fig.9c for the case of integrated MESFET pass transistor and in Fig.9d for an external HV JFET. One can observe that in the case of the HV JFET the output regulation is poor, due to the higher series resistance of the drift region, specific for the high voltage devices. However, our task is to demonstrate that the Voltage Reference is able to direct drive an external high power voltage controlled transistor MESFET or JFET as well.

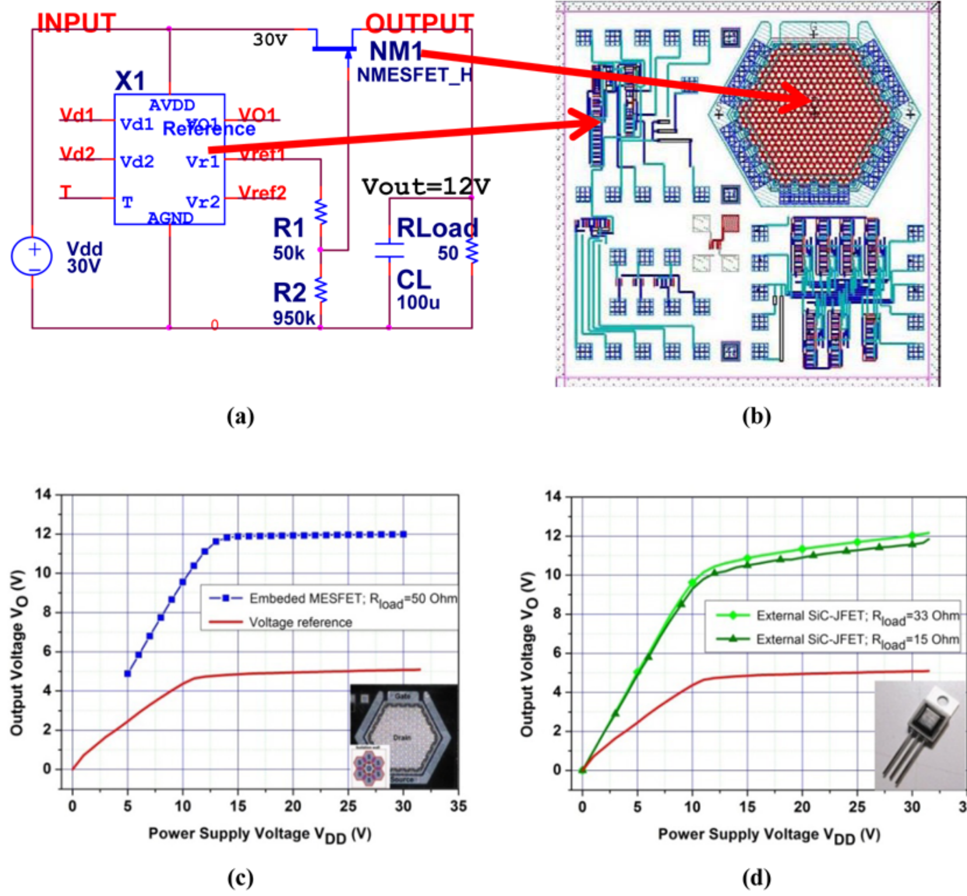


Fig. 9. (a) Demonstration of simple voltage regulator implemented with SiC voltage reference and SiC pass transistor, (b) Voltage reference and power pass MESFET as fully integrated application schematic, (c) output characteristics for using of the integrated SiC MESFET pass transistor, (d) output characteristics for driving an external high voltage SiC JFET pass transistor.

Figure 10 contains the electrical characteristics of the integrated power MESFET from the Fig. 9b. The output characteristics, the transfer characteristics and the blocking characteristics are shown in Fig. 10a to 10c respectively. Figure 10d shows a micrograph capture detail of the power transistor, which is embedded on the same chip with the Voltage Reference (see also Fig. 9b).

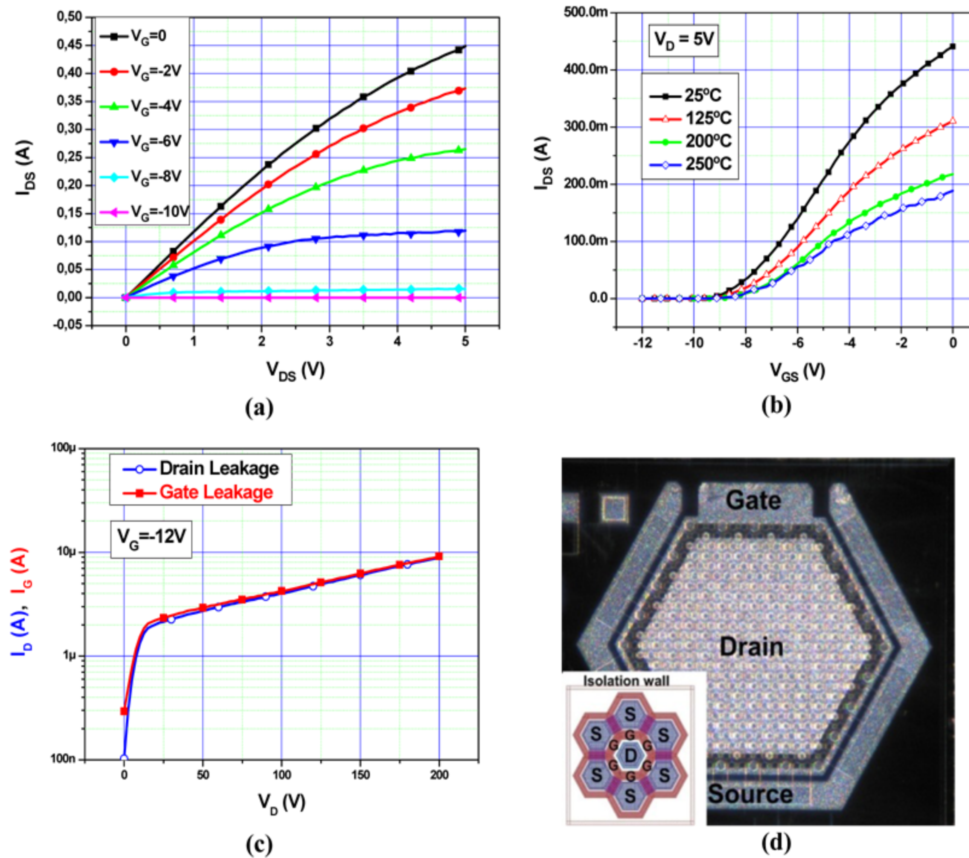


Fig. 10. Characteristics of the integrated SiC MESFET pass transistor:(a) Output characteristics; (b) transfer characteristic up to 250°C; (c) Blocking characteristic; (d) Micrograph capture of the embedded power MESFET and elementary hexagonal cell.

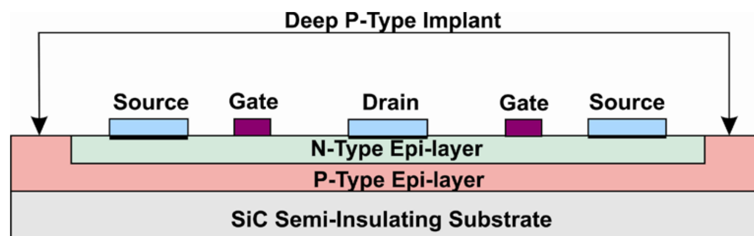


Fig. 11. Principle cross-section through an elementary cell of lateral power MESFET and the implanted isolation ring.

The elementary cell design of the power transistor is totally different from the one of the finger type MESFET used in the VR schematic. Externally, the power transistor is isolated by the same deep P type implanted walls as the finger MESFET,

but the gate is a closed loop design in hexagonal geometry (Fig. 10d). The elementary cell cross section of power MESFET is showed in Fig. 11. The deep P type implant reaches the P type epitaxial layer, creating an N tub. This tub is electrically isolated from the rest of integrated circuits by the reverse biased junction between the N tub and the P isolation walls. As inferred from Fig. 10d, the drain of the elementary power MESFET is surrounded by the hexagonal gate and six gate cells. The electrical contacts are distributed on three metal levels.

4. Conclusions

A brief analysis and experiments on the bandgap reference concept on the SiC was performed, demonstrating the voltage levels that are expected in the case of bandgap reference topology. The concept of bandgap reference is applicable not only for the silicon case, but also for SiC, the reference voltage level $V_{BGbip} = 3.17$ V, being close to the bandgap value EG=3.26 eV, in the case of using bipolar diode or transistors. It is also possible to obtain a bandgap-like circuit using Schottky diodes, in this case the reference voltage $V_{BGSch} = 1.44$ V. But up to the development of an integrated operational amplifier, this topology is not yet possible to be used for a monolithic integrated voltage reference.

However this work offers an early solution for the high temperature Voltage Reference with low drift on SiC. The voltage reference is an essential building block for further development of silicon carbide integrated circuits technology, mainly for SiC intelligent power application. Of our knowledge, this is the first reported Voltage Reference on SiC material built with MESFETs, and probably one of the first Voltage Reference with low temperature drift built on silicon carbide. This 4H-SiC IC Voltage Reference demonstrates experimentally a low drift over a wide temperature range and a high output level. The circuit is able to direct drive a SiC integrated power MESFETs or an external 3A high voltage SiC JFET. The main merit of this circuit is the simplicity of the schematic and technology that made possible the issue of the first monolithic thermal compensated Voltage Reference built on SiC. The Schottky gate technology of the MESFETs is based on the qualified high temperature stable and reliable Schottky contact, into the frame contract of the Space Mission Bepi Colombo [10]. A special planar finger-type MESFET was elaborated in order to achieve integrated circuits on SiC. The integrated in the circuit of temperature sensor block offers a simple way to implement the over temperature lock-out protection. Using the same schematic implemented with JFETs, we expect to nearly double the temperature range. The main limitation of the MESFETs schematic is the barrier sensitive gate leakage, much higher than the JFETs.

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