On the reset threshold voltage of ReRAM devices and its impact on the implication logic operation

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Abstract—ReRAM devices show potential for in-memory computing systems due to their capability to both store and process data via implication logic. This type of logic, which is typically implemented using the set transition, could offer reliability and performance advantage if implemented with reset switching of the device. However, the gradual transition of the reset makes it impractical. This paper presents the experimental observation of the reset transition sharpening as the initial ON state of the device is made more conductive and a simple explanatory model for this behavior.

Keywords—ReRAM; memristor; implication logic

1. Introduction

Borghetti et al. experimentally demonstrated [1] that a simple circuit with two passive resistive switches (memristors or ReRAM [2]) and a load resistor performs material implication (IMP) on the set switching - a universal Boolean operation together with the reset operation. When both ReRAM devices are initially OFF and the required voltage "clock" pulses are applied, device Q turns ON due to higher voltage drop across it. The IMP operation on set is equivalent to Q ← (NOT P) OR Q, see Fig 1a.

The IMP logic can also be implemented using the reset transition - the conditional switching only happens when both devices are ON - equivalent to Q ← (NOT P) AND Q. The reset IMP is more reliable since the device Q is not over-stressed, since the power is decreasing during the switching from ON to OFF. Having both set and reset IMPs could enable higher throughput and parallelism in computation.

However, typical bipolar oxide ReRAM has a gradual reset transition which represents a significant problem for the margins of the operation. Sharpening this reset transition would be beneficial for the reset implication logic.

This work presents the experimental observation of a reset transition sharpening based on the initial ON state of the device. A simple model for this phenomenon is presented.

2. Experimental results

The experimental results presented in this work were typical for a ReRAM device in a two□level stack with four metal□oxide devices (Fig. 1b). Al_2O_3/TiO_{2-x} active layers and Ti/Pt electrodes were used in the device fabrication. The substoichiometry of the TiO_{2-x} film was controlled by changing the oxygen:argon ratio in the reactive sputtering chamber. A planarization step after the fabrication of the bottom device ensured that the devices in both layers have similar characteristics and performance. The full details of the fabrication and electrical characterization are presented elsewhere [3].

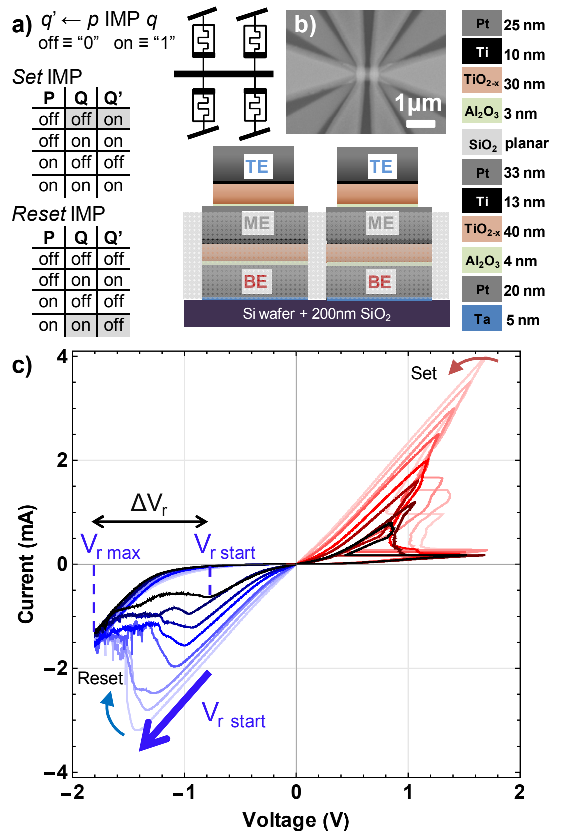

Fig. 1. Implication logic truth table (a) for ReRAM devices (b – SEM photo) with typical gradual reset (c) that sharpens with increasing initial ON state.

The devices were characterized electrically using an Agilent B1500 parameter analyzer. The ReRAM devices needed a one-time electroforming step, with forming voltages <3V. The devices in both layers present similar I-V characteristics. The set transition is relatively sharp, while the reset transition is more gradual.

As it can be observed from Fig. 1c, as the initial ON state of the device become more conductive, the reset operation is sharper.

3. Model

To model this behavior, we assumed an ideal memristor device with an R_{ON} resistance in series with an constant resistance (likely due to the line resistance, contact resistance, etc) as in Fig. 2. This model is characterized by the equation:

$$\overline{V}_{r\,start}(R_t) = \overline{V}_{rs}\frac{R_t}{R_t - \overline{R}_s} \qquad (1)$$

where the fitting parameters are V_{rs} (in V) which could be considered as the voltage at which the device starts resetting and R_s (in Ω) the internal series resistance of the device. For the analyzed devices, V_{rs} is fitted as 0.799V and R_s as 224 Ω in Mathematica 10. This method could be used to get an approximation of the internal series resistance and the threshold voltage.

As the initial device state is more conductive, the R_{ON} of the memristor device is smaller. More of the applied reset voltage will drop on the series resistor R_s, so a higher total applied reset voltage is needed for the device to switch. This model explains why as the initial ON state is more conductive, $V_{r\,start}$ for switching is higher in magnitude (Fig. 2a) and the ΔV_r decreases (Fig. 1b). A smaller ΔV_r equivalent to a sharper transition increases the operational margins and thus the reliability of the implication logic gate.

An ideal memristor (Biolek model [4] with Joglekar window [5]) in series with a resistor R_s was implemented in LTSpice (Fig. 2b). By varying the value of the series resistor, it is noticeable that a series resistor produces sharpening in the reset transition, in agreement with the experiments. Larger R_s leads to smaller ΔV_r, at the expense of extra power consumption.

4. Conclusions

In summary, we have presented experimental observation of the sharpening of the V_{reset} as the initial ON state of the device becames more conductive. We have explained these findings by a simple model. The sharpening of the reset transition has potential benefits for the implementation of ReRAM implication logic.

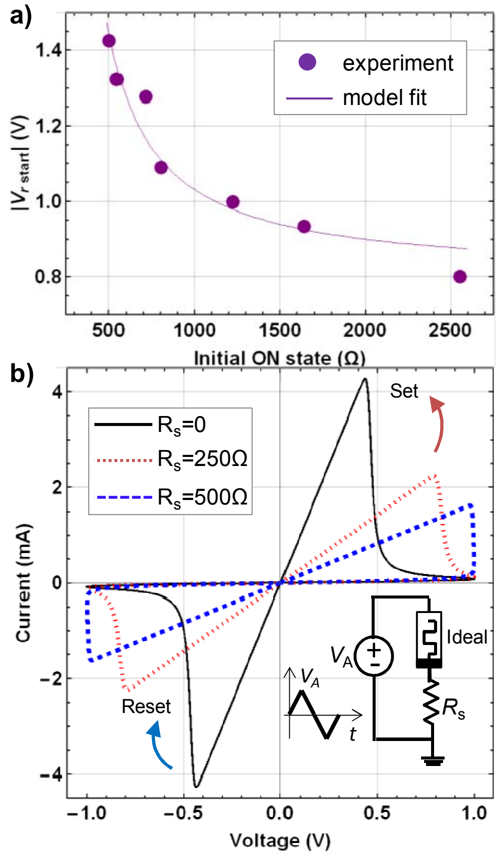

Fig. 2. The value of the reset voltage at which the device starts switching ($V_{r\,start}$) vs. the initial ON state, as extracted from Fig. 1b. The eq. (1) is fitted to the data with V_{rs} = 0.799V and R_s=224 Ω

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