Conductive through silicon via holes for RF applications

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Outline

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Manufacturing method

Process optimization

Gold electroplating

Conclusions

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Introduction

• Emphasis of the systems on chip (SOC) and in package (SIP) required the development of 3D encapsulation methods; a great efforts been made microelectronic devices miniaturization, higher and higher packaging densities being required
• Through-silicon interconnection technology is considered to be a critical and enabling technology for 3-D stacking of electronic and electro-mechanical systems

Manufacturing involve two problems: through wafer via holes manufacturing and holes filling with a conductive layer.

Via holes manufacturing methods: anisotropic wet etching, powder blasting, laser ablation, laser melt cutting or deep reactive ion etching (DRIE); geometries with aspect ratio between 1 and 20.

From all fabrication techniques DRIE shows its superiority in respect of pattern transfer and minimum dimensions – aspect ratio even bigger than 20 it is possible to achieve, while the accuracy will be provided by the photolithography.

Conductive layer / via holes filling:

- copper – critical advantage of being able to fill high-aspect ratio holes by electroplating
- polysilicon - heavily doped, conformal deposition by low-pressure chemical vapor deposition (LPCVD)
- the alternative is to use gold as conductive layer - poor adhesion to dielectrics and the need for barrier and/or adhesion layers

Our aim was to use gold as conductive layer; tapered walls – allow to deposit barrier and seed layer (CrAu) by PVD techniques

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Manufacturing method

• based on the possibility to change the process isotropy

Transition from one process type to another can be achieved by changing the plasma composition and can be performed during the same processing step.
By mixing the basic processes (anisotropic and isotropic) it is possible to obtain new shapes, unique, that cannot be obtained by other techniques.

DRIE processing main steps:
• anisotropic etching (Bosch process type) – to achieve the via depth
• isotropic etching – to enlarge via
• plasma oxygen (before isotropic etching) - to remove the passivation from the walls

Etching cycles are repeated until the opposite wafer surface is reached.

The via holes shape – strongly influenced by the number of anisotropic/isotropic etching cycles used and length of each etching step.

Size of the holes (diameter) is given by the initial etching window on one side, while on the opposite side will be greater, being influenced by the number and length of isotropic etching steps used.

Schematic view of the technological flow

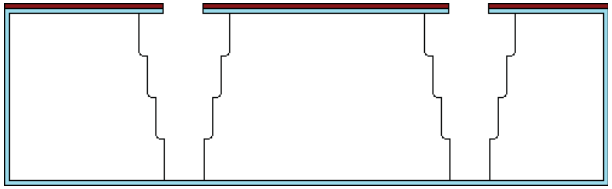
Thermal oxidation

Resist deposition and patterning; SiO2 dry etching

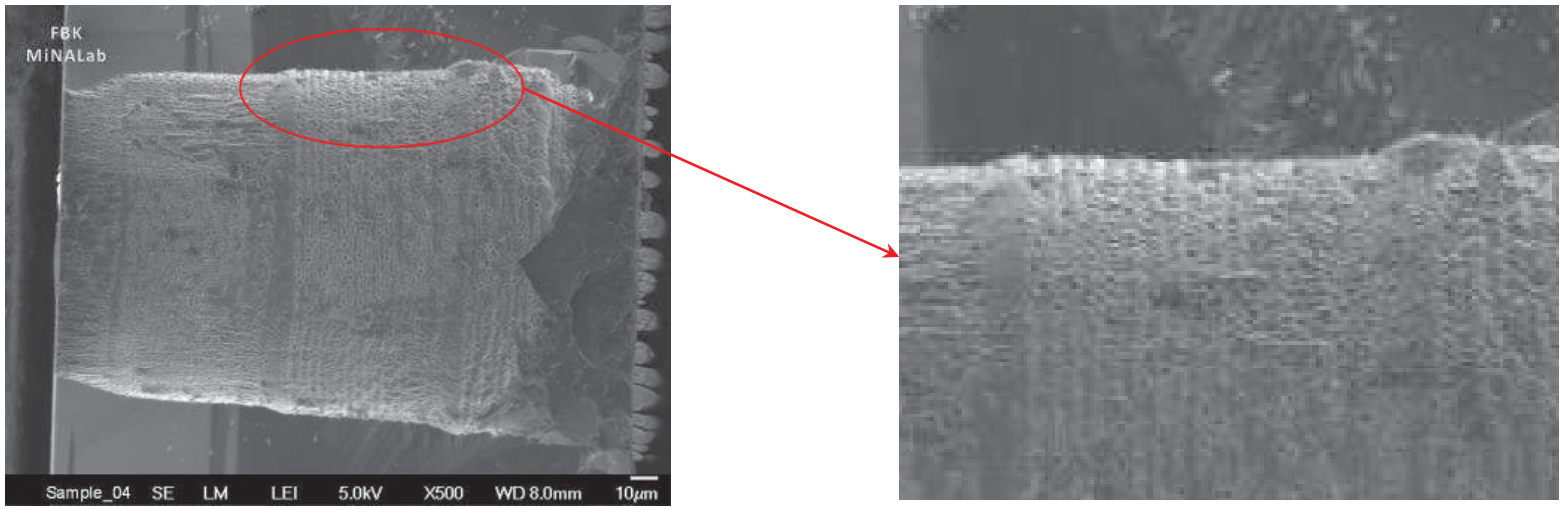
Anizotropic etching step

Isotropic etching step

New etching cycle



TWV manufactured by DRIE variable isotropy process



SEM photos of the manufactured TSVs using 200 microns thick wafers.

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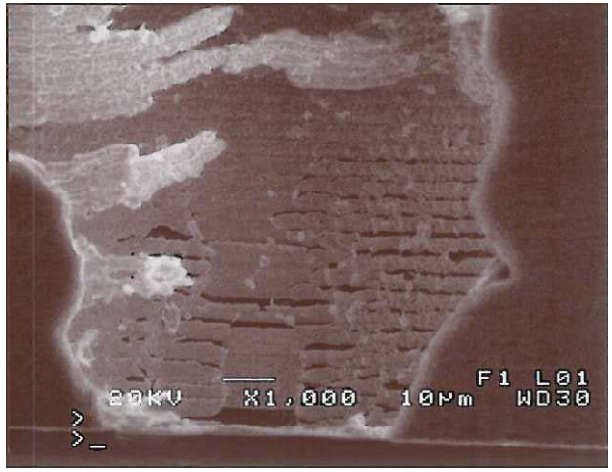
Process optimization

- rating of etching rate of each process type – anisotropic & isotropic
- wall roughness reducing by using various types of anisotropic etching recipes
- optimization considering depth attenuation

✓ARDE effect (Aspect Ratio Dependant Etching) – different opening etching sizes provide us extremely different etching rates; 20µm & 100µm diameter
✓ three different anisotropic etching recipes were used
✓ various types of wafers were used, with thicknesses between 200 and 500 microns

First optimization step
- etching windows - 100µm
- anisotropic etching → HER (High Etching Rate)
- measured etching rates:
  - anizotropic etchings ~17,33µm/min
  - isotropic etchings ~2µm/min.

After metalization

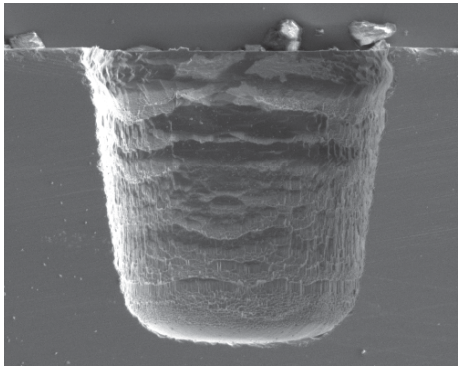


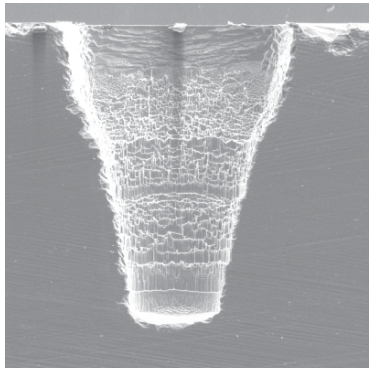
Second optimization step

- etching windows – 20µm & 100µm
- anisotropic etching recipes – SDE* & LR**
- targeted wall angles – 21.8°
- depth target – 200µm (for 100µm diameter etching windows)

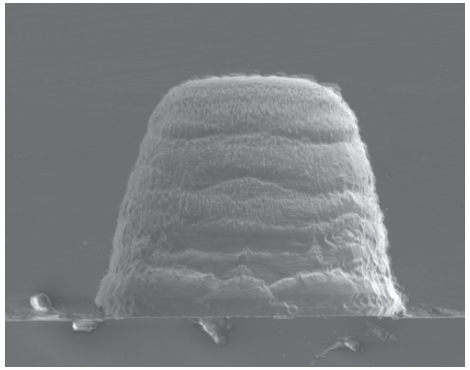
* SDE – Silicon Deep Etching (smaller gas flow/pressure and power; higher substrate bias)

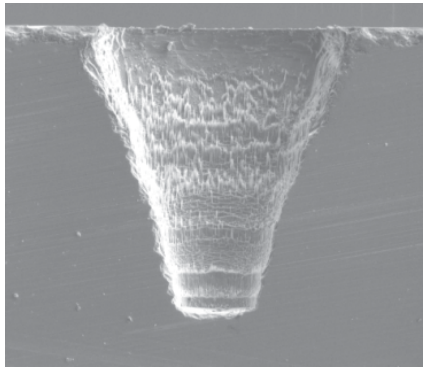
** LR – Low Roughness (gas flow/pressure and power greatly reduced)





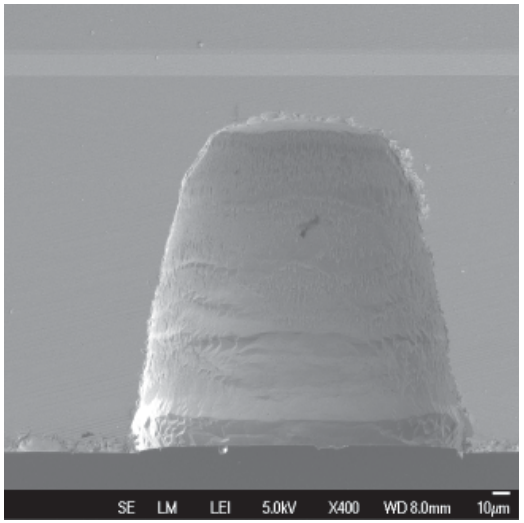
20µm and 100µm diameter cavities – SDE recipe

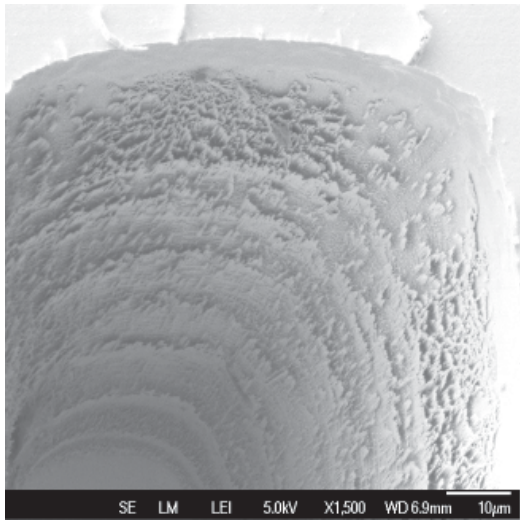




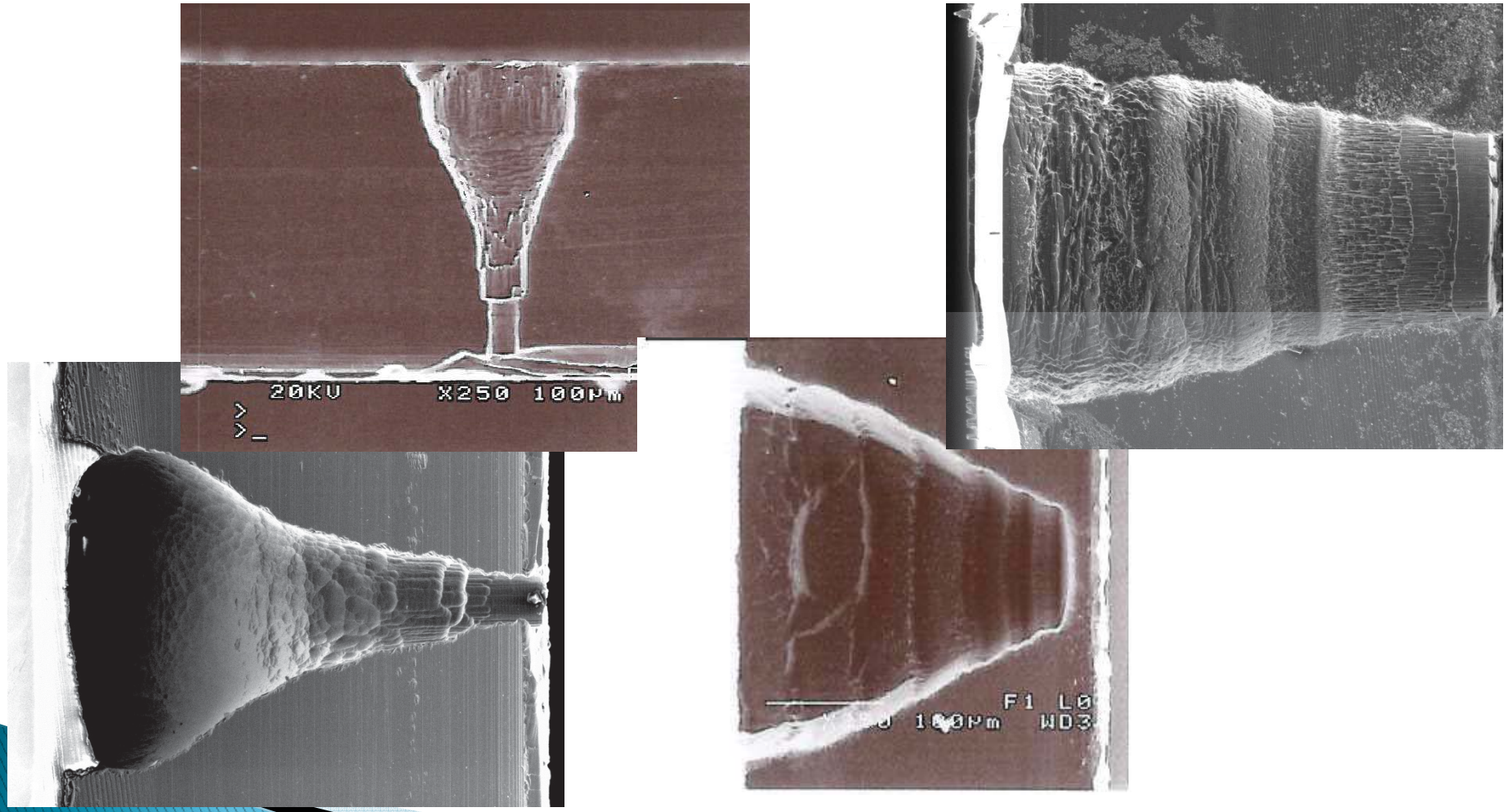
20µm and 100µm diameter cavities – LR recipe

- *depth → 160µm ÷ 200µm for 100µm diameter etching windows and 110µm ÷ 130µm for 20µm diameter, depending of anisotropic etching recipe*
- *lateral etching → ~48µm for 100µm and ~30µm for 20µm*
- *measured angles → 14° ÷ 18°*
- *for 20µm – etching rates smaller by 35% comparing with 100µm diameter etching windows*
- *very low roughness - not only the effect of changing the anisotropic etching recipe, but also due to longer isotropic etchings to obtain higher angles; nanometer peaks on the walls*





Last optimization step – 20µm & 100µm diameter etching windows; aspect ratio → up to 15:1; targeted angles → 11,3° (60µm) si 21,8° (120µm)



Measurements have revealed very good agreement between design and experiment .

	Mask diameter			
Parameter	20μm		100μm	
Target angle (lateral etching)	11.3° (60μm)	21.8° (120μm)	11.3° (60μm)	21.8° (120μm)
Bottom size	~25μm	~27μm	~140μm	~100μm
Top size	~134μm	~190μm	~252μm	~330μm
Measured angle	~10.3°	~15.2°	~10.57°	~20.97°
Error	~9.17%	~31.7%	~6.67%	~4.17%

DRIE variable isotropy process for TWV manufacturing allow a very good control of the wall angles, it is reiterative, process optimization being easy to achieve, demanding minimal resources and a short time.

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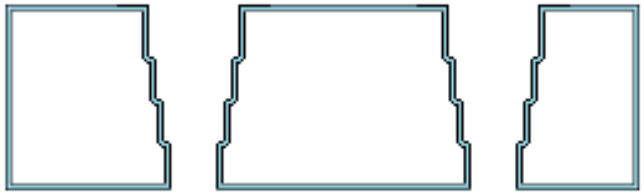
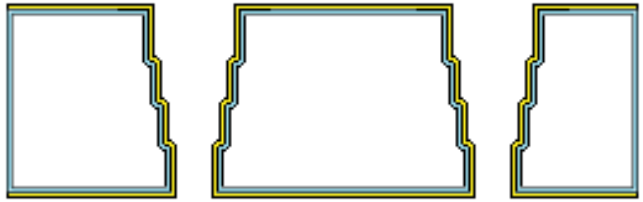
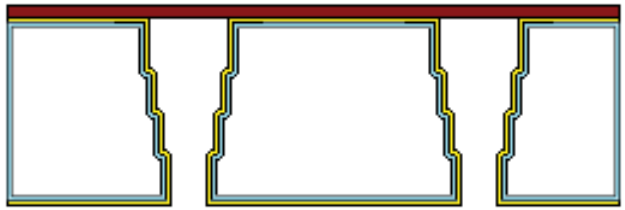
Conductive TWV manufacturing using gold electroplating



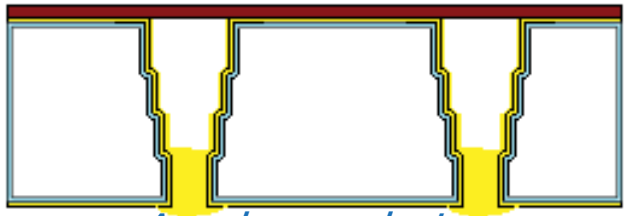
Resist removing, SiO2 etching and thermal oxidation



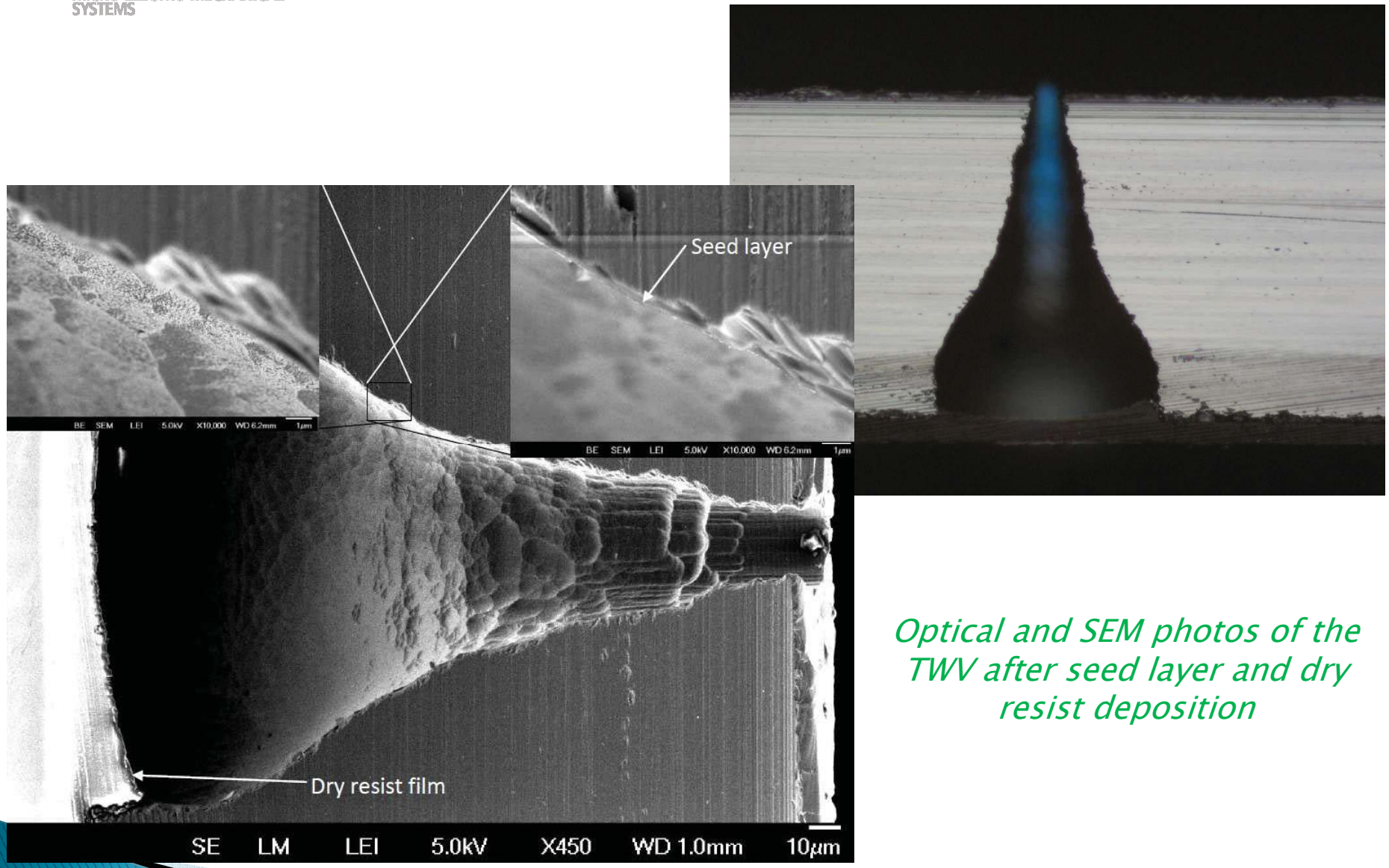
TiAu deposition, e-beam (both sides)



Dry resist deposition



Au electroplating



Optical and SEM photos of the TWV after seed layer and dry resist deposition

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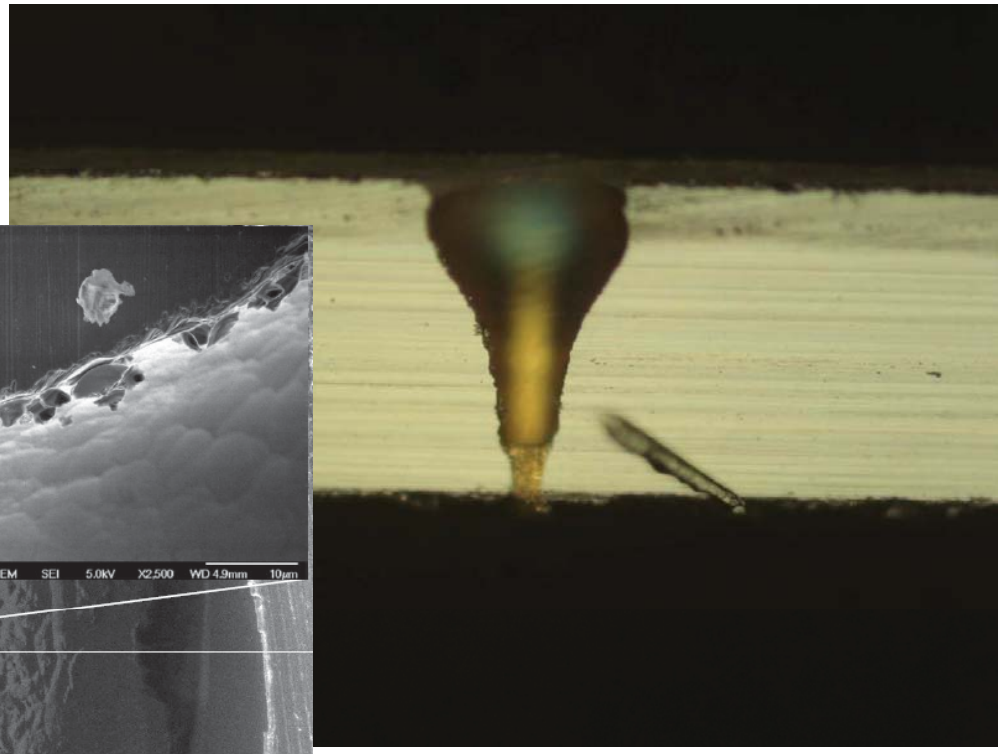
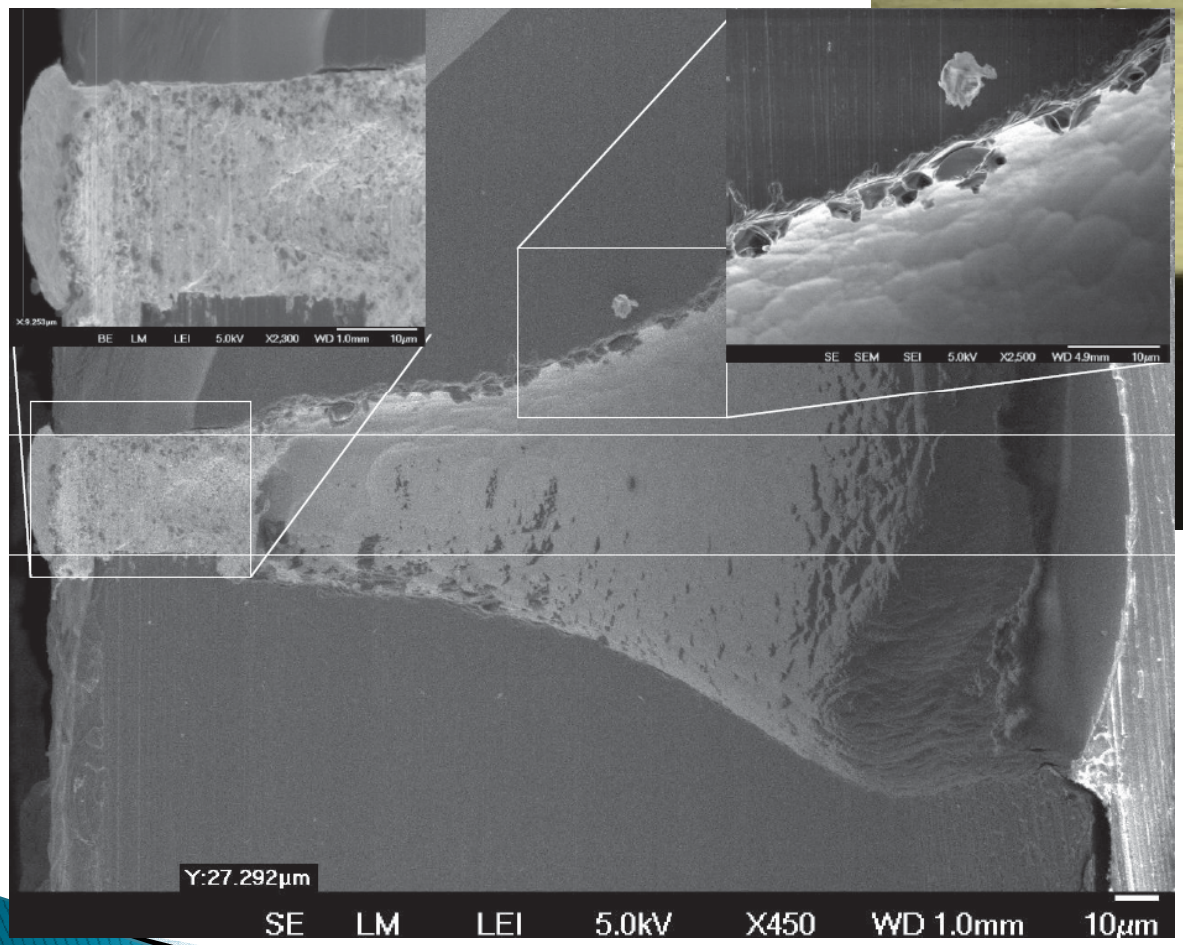
Optical and SEM photos of the TWV after Au electroplating





Measurements performed showed that the whole narrow part was filled on a depth between 50 and 70µm for all via's.

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CONCLUSIONS

- a new method to obtain conductive through wafer via's was presented
- tapered TWV were manufactured by DRIE using a variable isotropy process, allowing a very good control of the wall angles
- a very good coverage of the via walls by seed and barrier layers was demonstrated
- gold electroplating was used to fill the narrow part of the via's on a depth of at least 50µm
- obtained structures, even partially filled, allow a subsequent processing of the wafer at least on one side.