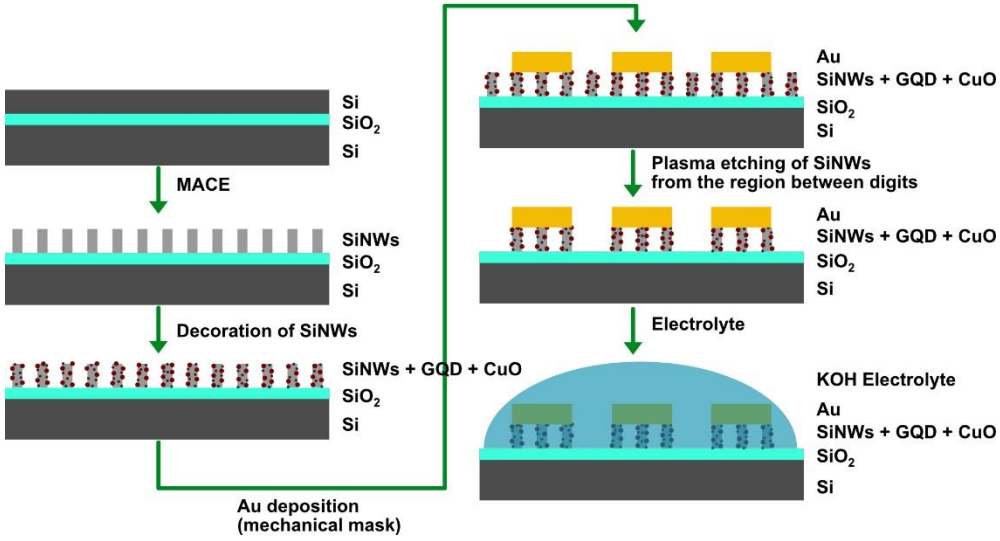
Stage 3 - 2023 *Fabrication of 3D nanostructured MSC test devices*

The proposed objectives and tasks in this stage were achieved as follows:

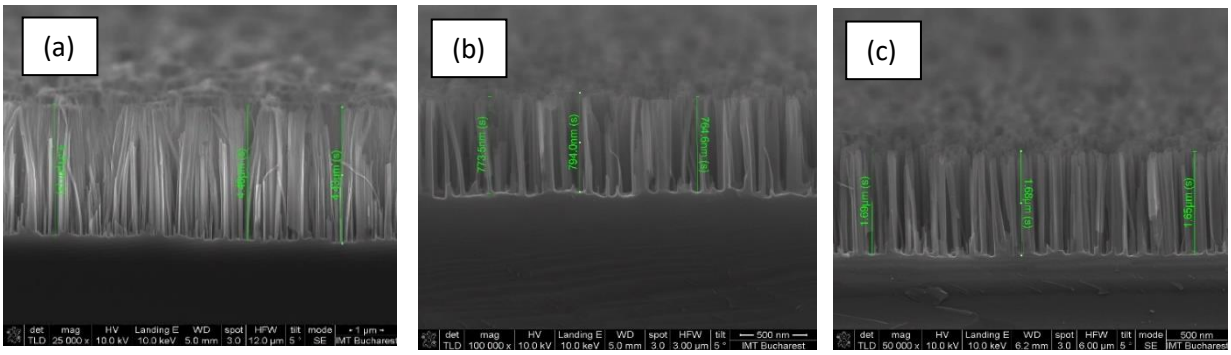
1. Processes' optimization; selecting the process flow enabling further CMOS integration – Act 3.1.

Within this activity, the technological processes of manufacturing 3D structures of planar micro-supercapacitors with high height/surface ratio on SOI substrate were optimized. Figure 1 schematically shows the technological flow followed, containing the main technological stages:



Technological process flow

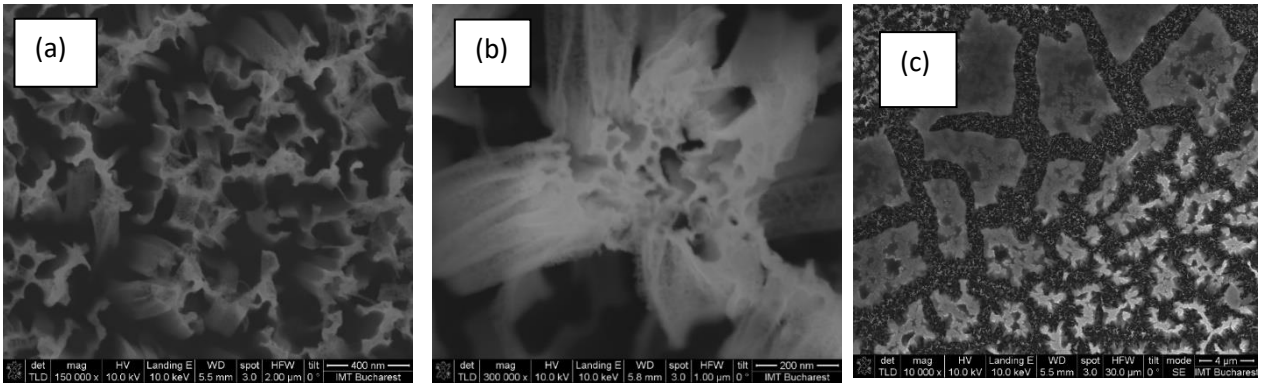
As can be seen, the first step was to obtain a 3D platform on the initial SOI substrate by adapting the classic process of metal assisted chemical etching (MACE) of Si nanowires - **E2**. SOI wafers (Ultrasil LLC, USA), type P, with orientation (100) and two types of resistivities of the device layer, 0.005-0.02 Ωcm, and 5-10 Ωcm, respectively, were used for the fabrication. After being washed in acetone, isopropyl alcohol and deionized water for 10 minutes each, the wafers were subjected to a metal-assisted chemical corrosion process, being inserted into a Teflon vessel with 80 ml of a solution containing 12.4 ml of HF 50%, 67.6 ml deionized water and 0.815 g $AgNO_3$.



SEM imagines of SiNWs/SOI wafers with (a) 5-10 Ωcm, (b, c) 0.005-0.02 Ωcm, respectively, device layer resistivity.

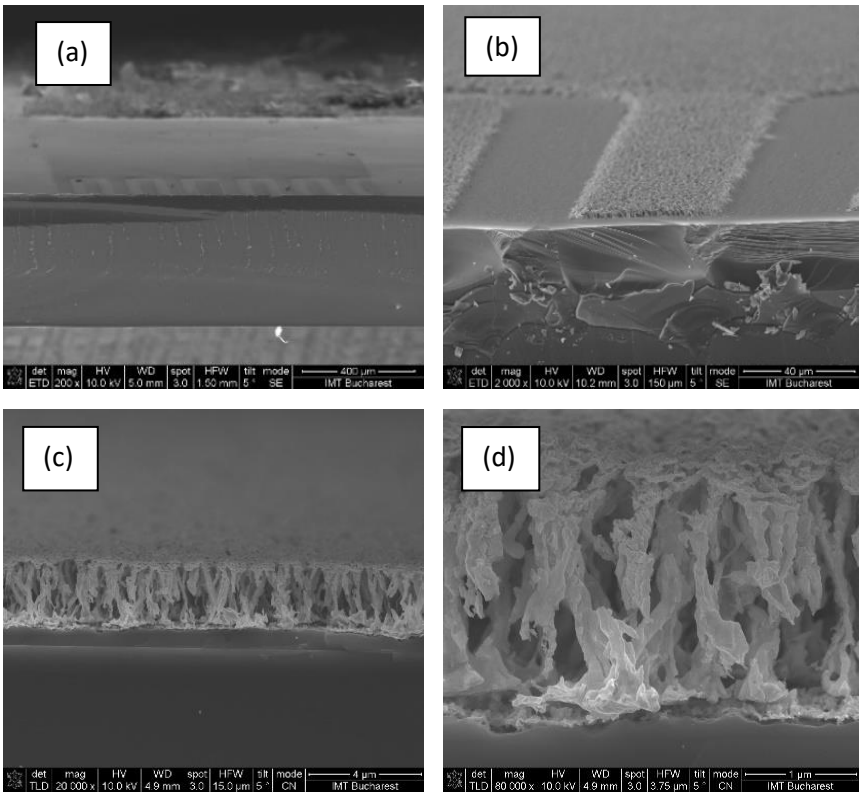
After preparation, the obtained SiNWs were treated for 2 minutes in a solution of hydrofluoric acid, HF 50%, for their hydrogenation, followed by abundant rinsing with deionized water and drying with nitrogen. The decoration with

metal oxide nanoparticles, CuO NPs and GQDs, was achieved by immersing SiNWs in the aqueous solution of copper chloride ($CuCl_2$) with a concentration of 0.1 M, for different time intervals, respectively, 5 and 8 minutes. The GQDs solution was dispersed in-situ during the formation of CuO NPs.



SEM images SEM of SiNWs/SOI decorated with CuO NPs and GQDs.

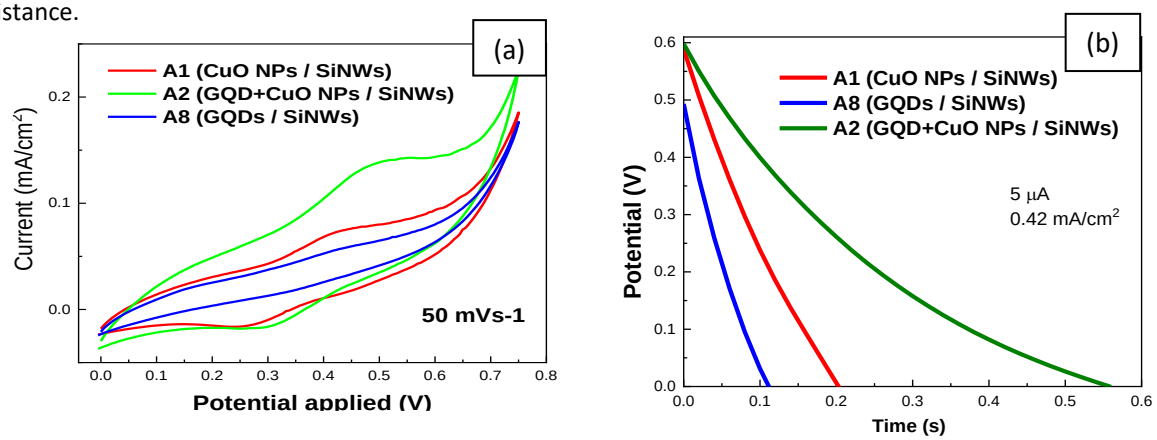
The interdigitated electrodes of the metal collector were fabricated (E4/fig. 1) using mechanical masks where the thickness of a digit and the space between them was 50 µm, and the active area was 1.9 mm^2, small enough to be integrated later in complex systems that can be used in IoT applications. The silicon nanowires between the electrode fingers were etched (E5/fig. 1) using a reactive ion dry corrosion (RIE) process. The etching aim was to obtain a tank for electrolyte that can easily reach the areas with active elements under the electrodes.



SEM images of the 3D - IDE structure on SOI

2. Complete characterization of the experimental structures - identification of charge transfer mechanisms in the obtained heterostructures. – Act. 3.2

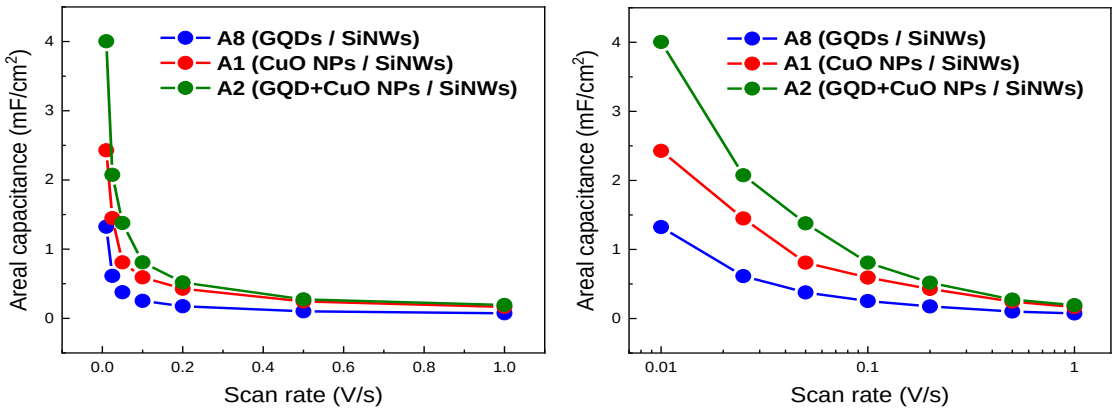
In order to evaluate the performance of the obtained planar micro-supercapacitors, standard electrochemical measurements were performed for each test structure using 1M KOH electrolyte. The advantage of using the alkaline electrolyte KOH in relation to other organic electrolytes is mainly given by the higher ionic concentration and lower resistance.



Comparison of the CV profiles obtained at a sweep rate of 50 mV/s for the 3 supercapacitors (a) and respectively of the discharge curves recorded at a current of 5 μA (b).

A substantial increase in current is observed when the 2 components are put together. On the one hand, the excellent mobility of the electrons in GQDs increases the conductivity of the active layer and greatly facilitates the transport of charges through the active layer.

Compared to graphene, GQDs have a higher specific surface area, more active surface sites and more accessible edges, which allow full accessibility of ions and their adsorption/desorption. These properties are highlighted by the profile of the recorded discharge curves (Fig b), where it is observed not only a much longer discharge time for the all assemble, in relation to each individual component, but also a more improved ohmic drop, in accordance with the results reported in the case of using CuO capsules decorated with GQDs as active material.



Specific areal capacitance

Thus, the GQDs-CuO hybrid layer increases the charge storage performance because by covering the SiNWs with GQDs, the porous morphology is maintained and implicitly, the electrical conductivity of the electrodes is improved.

First of all, it should be emphasized that the obtained values for the specific capacity are very good, higher than those reported for micro-supercapacitors with interdigitated electrodes. Regarding the evolution of the specific capacity with the increase of the scanning rate, a decrease of it is observed with the increase of the rate, due to the fact that the access of the ions to the inner region of the electrode is limited with the time decrease in a cycle.