Design, modeling and simulations of the micro and nanostructures MEMS/MOEMS
Institute of Electron Technology, Warsaw, Poland
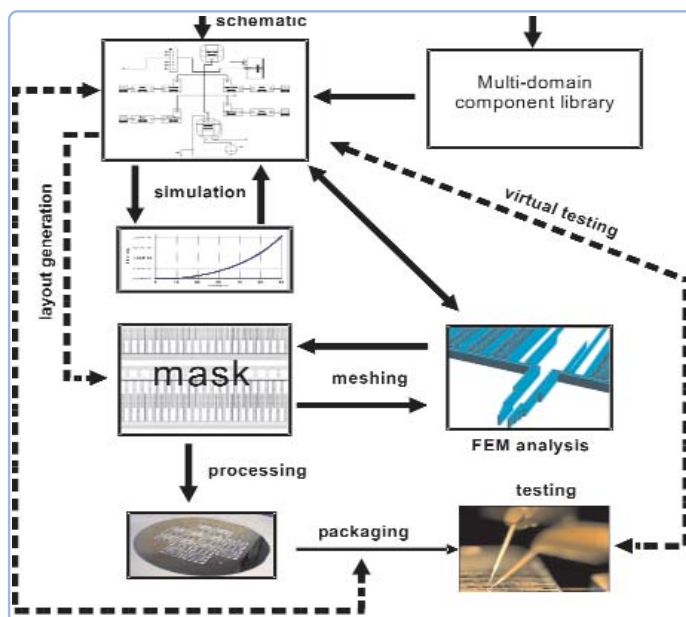### Division of Silicon Microsystem and Nanostructure Technology

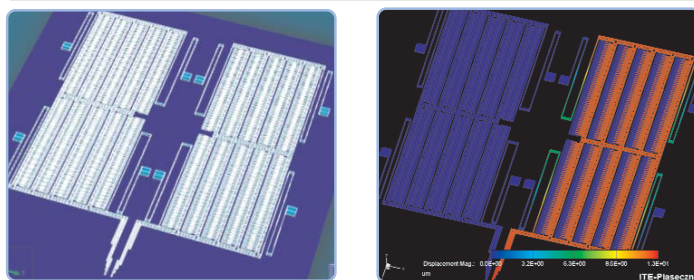Fig.1 Flow chart describing modern MEMS design, modeling and analysis.

Fig.2 3D-model of silicon microgripper with comb-drive and simulation results.

Modern methodology of MEMS design being extensively used at ITE is based on a system-level, top-down MEMS design process. The objectives of this method are to optimize the function of the devices and to minimize development time and cost by avoiding unnecessary design cycles and foundry runs (Fig.1).

Behavioural modelling of MEMS structures.
Instead of using a layout-drawing tool to create a 2D model, high-level design techniques use a graphical schematic capture tool to position and connect the model symbols that represent functional blocks (masses, plates, electrodes or micro fluidic parts) with underlying analytical formula.

Advanced techniques for MEMS/MOEMS/CMOS modeling. Very important issue is a possibility of simultaneously co-simulation of MEMS and IC unit. For MEMS structures integrated with integrated circuit controls the unit idea of Hardware-In-The-Loop basing on co-simulation using signal flow simulators is particularly promising. The goal is to verify whether the hardware and control algorithms work together without failure. In ITE we are using for co-simulation Architect module from CoventorWare and Simulink.

Finite Element Method for MEMS/MOEMS modeling and simulation.
Analyzer (module of CoventorWare) allows to use FEM analysis for multi domain simulation (electrical, mechanical, thermal, electrostatic, piezoresistance, microfluidic etc. and it's combination e.g. thermo-mechanical) of the micro and nanostructures. Example based on electrostatic driven microgripper with comb-drive modelling shown on Fig. 2.

Virtual manufacturing of MEMS structures.

Designers developing MEMS and other IC devices quickly and cost effectively need detailed 3D models to help visualize each step of the fabrication process. Visualization allows designers to see what happens during material deposition and etching and catch errors before building an actual mask or prototype.

The process emulation approach at ITE uses 3D numerical simulation to produce highly accurate models of the effects of chemical reactions involved in fabrication. SEMulator3D-Memulator/Etch3D™ environment uses voxel (3D-pixel) algorithms to furnish the accuracy of physical process simulation and the speed and capacity of process emulation techniques (PECVD, LPCVD, deposition, etch wet, anisotropic, KOH/TMAH, CMP, oxidation, diffusion etc…).

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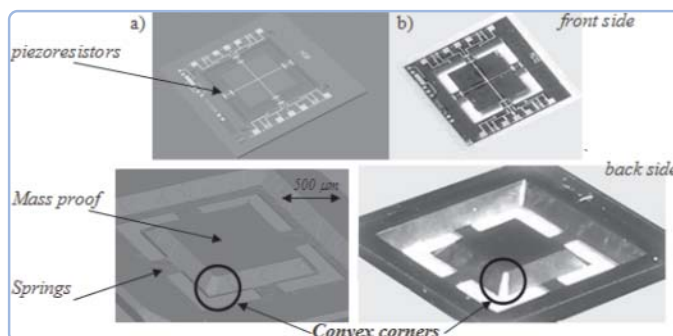*Authors of this paper: "T. Bieniek, P. Janus"*

Fig. 3 Bulk-micromachined silicon piezoresistive accelerometer a) simulated, b) manufactured.
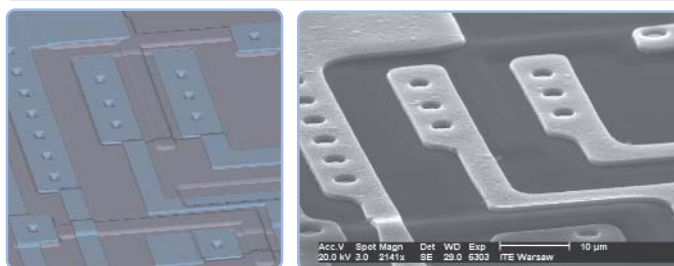

Fig. 4 Emulation of the ITE CMOS fabrication process (left) and SEM image of the structure (right).