TUNELLING LEAKAGE CURRENT CHARACTERIZATION OF SILICON OXIDE AND HIGH-k DIELECTICS FOR ADVANCED SEMICONDUCTOR DEVICES

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Abstract: *The continuum down-scaling lead the field-effect transistors in the nanometre region with devices and structures characterized by high doping drains/sources and thin insulating layers. When the thickness of the layers attends 2nm or less, the coupling between the semiconductor channel and the gate can't be neglected. A correct quantum-mechanical model must correct evaluate the channel charge distribution and the leakage current flowing between the gate and the channel through tunnelling.*

INTRODUCTION

➢The continuous decrease of ultra-large-scale integration dimensions determines that SiO_2 gate dielectric attends critical dimensions of tens of Å and reaches fundamental limitations in preventing current leakage from the gate into the channel.

➢One possible solution is to replace SiO_2 with higher permittivity insulator materials. Among the promising candidate materials investigated are HfO_2, $HfSiO_4$, $ZrSiO_4$, La_2O_3 and Y_2O_3.

RESULTS

For numerical simulations we used the ATLAS devices simulator software package from Silvaco and the main structure is presented in fig. 1. The calculated gate current is presented in fig. 2 and the capacity from gate to substrate in fig. 3, function of polysilicon doping concentrations $10^{19}cm^{-3}$, $10^{20}cm^{-3}$ and $10^{21}cm^{-3}$. Using the barrier height of 3.1eV, substrate doping $5x10^{17}cm^{-3}$, effective silicon oxide mass of $0.5m_o$ and donor poly doping $6x10^{19}$ the results of short computation iterative approximation of silicon oxide current gate density, fig. 4, was in good agreement with experimental gate current density curves presented in [9]. The performances of SiON like gate dielectric are better than SiO_2 as in fig. 5, according with simulations and ITRS. Comparing the calculated data with gate leakage current through Al_2O_3 high-k dielectric stacks presented in [12] a good fit was obtained, fig. 6.

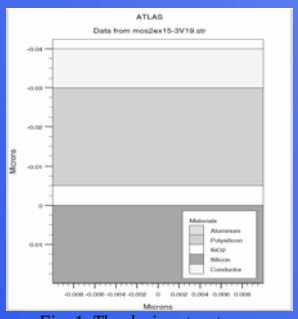

Fig. 1. The device structure.

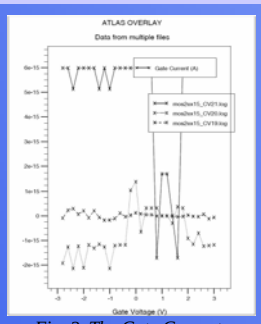

Fig. 2. The Gate Current.

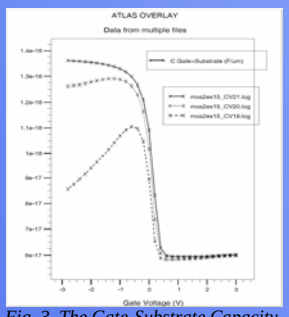

Fig. 3. The Gate-Substrate Capacity.

THE ITERATIVE APPROXIMATION METHOD

Using the geometrical approximation of Si band bending in inversion the energy level is:

$$E_{z,ij} = \left(\frac{\hbar^2}{2m_{z,i}}\right)^{1/3}\left(\pi q F_{ef}\frac{3}{2}\left(j+\frac{3}{4}\right)\right)^{2/3}$$

and the subband charge is: $q_{ij} = \frac{2E_{z,ij}}{3qF_{ef}}$

where F_{ef} is the $E_{z,ij}$ corresponding effective Electric field. Then the inversion charge is:

$$q_{inv} = \sum_{i,j} q_{i,j}\frac{N_{i,j}^{(2D)}}{N_{inv}}$$

and the total silicon surface bending:

$$\Psi_S = \Psi_D + q\frac{N_{inv}q_{inv}}{k_{Si}\varepsilon_0} + \frac{k_B T}{q}$$

Using the charge boundary conditions the equations can be iteratively solved to attain the convergence in the next sequence:

1- Guess the initial N_{inv}, Ψ_S and Ψ_D
2- Consider charge boundary condition Ninv-bc
3- Iterate Ψ_S with condition $N_{inv}(\Psi_S)/_{Ninv-bc} \rightarrow 1$
4- Iterate Ψ_D with condition $\Delta\Psi_D \rightarrow 0$
5- Compute the potential distribution
We have possible loops from out to input, of step 3 and 4 and from out of step 4 to input of step 3.

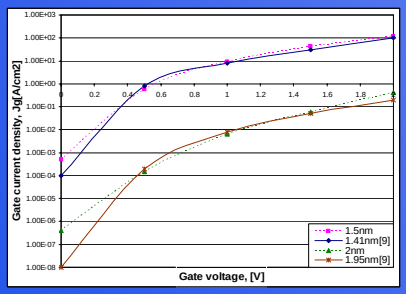

Fig. 4. Silicon oxide gate current density calculated (1.5nm and 2nm) and experimental curves presented in [9], (1.41nm[9] and 1.95nm[9]).

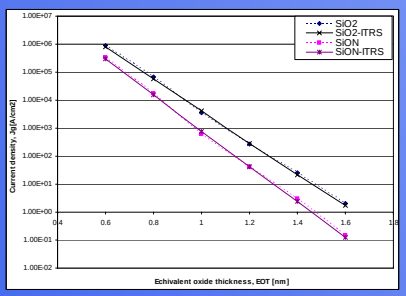

Fig. 5. Simulated and ITRS tunnelling current gate leakage in inversion channel for oxide and oxynitride at Vg=1V.

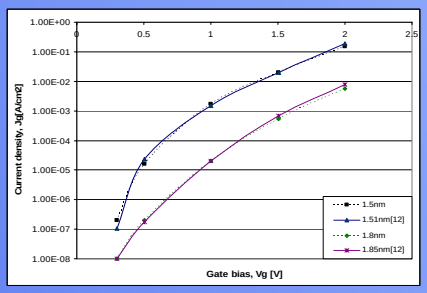

Fig. 6. Calculated data and experimental gate leakage currents [12], for Al_2O_3 high-k stacks.

CONCLUSIONS

➢The iterative method calculate the 1D MOS structures main electric parameters based on approximation of effective field function of doping parameters.

➢The main application is to calculate the direct tunnelling current due to the thin oxide layers and is extensible to high-k dielectric stacks in order to study the influence of several material parameters like the impact of layer thickness on gate leakage and the approach of gate stack scalability.

➢The increase of dielectric constant to 7 reduce the leakage current with 4 order of magnitude, like in fig. 5 and 7 for 1V gate bias and 1.5nm thickness.

➢Other simulations show that the leakage current decrease significant when the interfacing oxide is completely eliminated and future works will be focus of other high-k dielectric stacks like HfO_2, $HfSiO_4$, $ZrSiO_4$, La_2O_3, and Y_2O_3.

[9] N. Yang, W. Henson, J. Wortman, "A comparative study of gate dielectric tunnelling and drain leakage currents in n-MOSFET with sub-2-nm gate oxides", *IEEE Trans. El. Dev.* 47(8), pp. 1636, 2000.
[12] D.A. Buchanan,.. "80 nm poly-silicon gated n-FET with ultrathin Al2O3 gate dielectric for ULSI applications", *IEDM Tech. Dig.*, pp. 223-226, San Francisco, 2000.

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