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Two Device Screen Grid Field Effect Transistor Logic

Y. SHADROKH[1], K. FOBELETS[1], J. E. VELÁZQUEZ-PÉREZ[2]

[1] Electrical Engineering Department of Imperial College London, Exhibition Road, SW7 2BT London, UK
[2] Applied Physics Department of the University of Salamanca, Edificio Trilingüe, Plaza de la Merced s/n, E-37008 Salamanca, Spain
E-mail: y.shadrokh@imperial.ac.uk

Abstract. The Screen-Grid Field Effect Transistor (SGrFET) is an oxide-gated FET with a novel 3D gating configuration made of cylinders perpendicular to the current flow in the channel resulting in a radially extending electric field. The multiple gate finger design of the SGrFET not only lends itself to excellent control of short channel effects but can also be exploited in compact logic applications with a reduced number of devices per gate. In this report TCAD results of both the DC and transient performance of double-gate row SGrFET logic are presented. The SGrFET inverter logic gives ps rise times and large noise margins of up to 400 mV for 1 V supply. NAND, NOR and XOR logic can be obtained using only two n-type SGrFETs.

1. Introduction

As CMOS is scaling down with the aim of increasing operation speed and decreasing device area, the need for better control of the channel by the gate has driven research towards devices with multiple gate configurations. Different types of multiple gate FETs have been proposed of which the finFET with a 2, 3 or even 4 gate configuration is the most popular. Amongst the FETs with other multiple gate configurations is the Screen-Grid Field Effect Transistor (SGrFET) [1]. As the finFET, the SGrFET is defined on SOI (Silicon-On-Insulator), but its gating approach is completely different as can be seen in Fig. 1. No fins are needed as the SGrFET is planar. The gate consists of oxide cylinders (fingers) with a poly-Si or metal core. These fingers are placed perpendicular to the current flow in the channel. Different gate

configurations are possible, as explained in [1] but the most straightforward one that also gives excellent control on sub-threshold slope and drain induced barrier lowering (DIBL) is the two gate row configuration shown in Fig. 1. Increasing the current drive can be obtained by widening the device (and accordingly expanding the gate's grille), but unlike in conventional SOI technology the increase can also be obtained by increasing the body height without any detrimental effect to the gate control (DIBL, Short-Channel Effect (SCE), ...). Highly doped source and drain areas are located at both sides of the device and have the same width as the device, avoiding contacting problems to small areas. For optimum performance the channel doping is low to un-doped in order to preserve high mobility values and of the same doping type as the contact regions unlike traditional MOSFETs. The device operation is essentially based on the control of the carrier concentration between the gate fingers in the first row (the one closer to the source contact). The main role of the second row of fingers (the one close to the drain contact) is to screen the electrical action of the drain on the above mentioned carrier concentration, therefore the second row controls the amount of DIBL and other short channel effects (SCE) in downscaled SGrFETs. The SGrFET performs best in sub-threshold and weak inversion, in these regimes high mobility values can be expected due to reduced surface scattering because the carriers flow away from the cylinder walls.

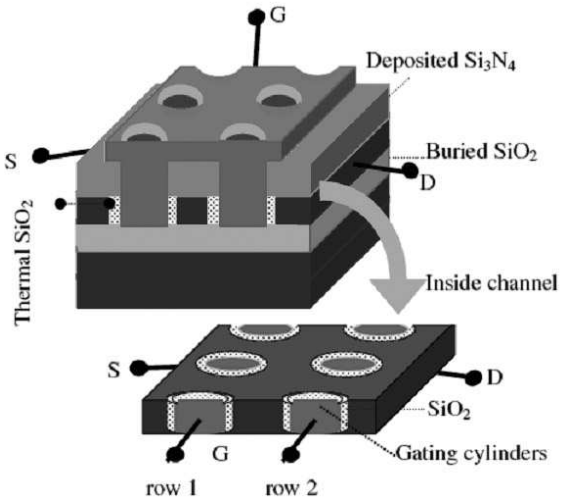

Fig. 1. Schematic configuration of a SGrFET with two gating rows, each consisting of 1 whole and 2 half gate cylinders. The top gate contact connects all gate cylinders in a single gate contact configuration.

Table 1. Device type as a function of work function

Device Type	V_{th} [V]	Metal Work Function [V]	Example of Gate Contact
n-SGrFET	0.44	4.8	Gold
p-SGrFET	0.3	4.8	Gold
n-SGrFET	–0.2	4.10	Aluminum

The threshold voltage of the SGrFET can be controlled, as in finFETs, via an appropriate choice of the gate workfunction, Table 1 shows the threshold voltage (V_{th}) values for two different gate metals.

2. DC analysis

The split-gate configuration of the SGrFET, where gate row 1 and 2 are not interconnected by the top gate contact, lends itself ideally for mixing and single device logic. This increased functionality of the SGrFET can be exploited for digital applications by applying synchronous or asynchronous voltages on the two gate finger rows.

For the simulations, in 2D, we have used Medici^{TM} [3]. 2D simulations are done on the cross section plane from source to drain parallel to the semiconductor/buried oxide surface. The hydrodynamic (HD) model has been used for DC simulations as the length of the active region is under a quarter micron, nevertheless the DC results obtained from drift-diffusion (DD) and HD models were similar. According to this, the DD model was used for transient analysis in order to save CPU time and prevent the appearance of convergence problems. The gate oxide thickness is $t_{ox} = 2$ nm, the source-drain distance $L_{SD} = 240$ nm, the diameter of the gate cylinders $L_O = 50$ nm and the distance between the outer edges of the gate cylinders within one row $L_c = 50$ nm. Where necessary the SOI body thickness is assumed to be 100 nm. For the DC evaluation of the split-gate performance an n-type SGrFET is used with un-doped channel area (N_D=10^{15} cm^{-3}) and highly doped drain and source regions (N_D=10^{19} cm^{-3}). In order to enhance the calculation speed one unit cell with four half gate circles is used, similar to [1]. N unit cells will give N times the current drive of 1 unit cell, all other performance parameters remain unaffected. The width of the unit cell in the simulations is thus $W_u = 2{\times}L_O/2{+}2{\times}t_{ox} + L_c = 104$ nm, unless otherwise stated.

Figure 2 shows the DC transfer characteristics for the split-gate functioning of the n-SGrFET. In these simulations the voltage of one gate row (with reference to Fig. 1: gate row 1 = G-S, gate row 2 = G-D) is kept constant at a high (H = 1V) or low (L = –0.3 V) voltage level whilst the voltage on the other gate row changes gradually between these two value. The source-drain voltage is kept at $V_{DS} = 1$V. The threshold voltage of the device when all gates swing between H to L is $V_{th} = 0.4$ V.

The values for the high and low gate voltage are those for which the device is respectively ON and OFF, and are given by [2]:

$$\begin{aligned} V_{ON} &= V_{DD} + V_{th} \\ V_{OFF} &= -V_{th} \end{aligned} \tag{1}$$

When one of the gate rows is kept at OFF, the drain current is very low ($I_{OFF} <$ $< 1.210^{-13}$ A/μm) and the sub-threshold slope, S, is very high ($S > 158$ mV/dec). This is a result of the efficiency of the pinch-off of the channel with one single gate row. Opening of a part of the channel region by increasing the voltage on the other gate row does not allow the SGrFET to switch on. However, when one of the gate

rows is ON, currents increase and S decreases to near optimal values. The threshold voltage shifts between H and L state, creating the possibility for single device logic. Table 2 summarizes these results.

Table 2. DC Parameters of Split-Gate SGrFET operation

Configuration	V_{th} **(V)**	S**(mV/dec)**
V_{G-D}=H, V_{G-S} swings	0.4	68.40
V_{G-D}=L, V_{G-S} swing	0.16	158.2
V_{G-S}=H ,V_{G-D} swings	0.3	80.20
V_{G-S}=L, V_{G-D} swings	0.17	186.9
V_G swings	0.4	61

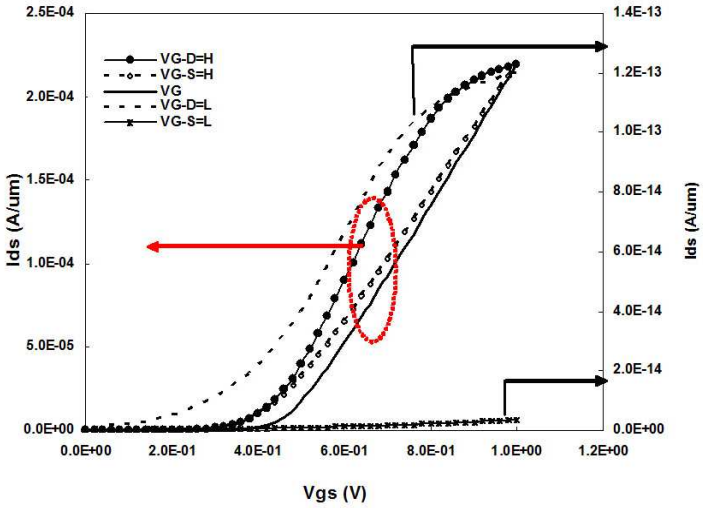

Fig. 2. Transfer characteristics of the DC sweep of one gate row with the other gate row voltage constant. V_{DS} = 1 V. (—●—) V_{G-D} = H, V_{G-S} swings (—•—) V_{G-D} = L, V_{G-S} swings (—◈—) V_{G-S} = H V_{G-D} swings (—⋆—) V_{G-S} = L, V_{G-D} swings, (———) V_G swings (single gate contact configuration).

3. Analysis of logic circuits

In this section we first investigate the SGrFET in classical complementary and all-n-FET (Enhancement-Depletion, EDMOS) inverter circuits where the same voltage is applied to both gate rows. Then a two-device NAND, NOR and XOR are also investigated where the split-gate configuration discussed in section II is exploited to make the circuit more compact. Both DC and transient analysis will be presented.

3.1. Inverter circuits

Two possible configurations are studied, the complementary C-SGrFET and the n-SGrFET EDMOS inverter. “ON” and “OFF” gate voltages are as defined in Eq. (1):

$V_{ON} = 1.4$ V and $V_{OFF} = -0.4$ V for the n-type and $V_{ON} = -1.3$ V and $V_{OFF} = 0.3$ V for the p-type SGrFET. The load in the n-SGrFET inverter is a depletion mode n-SGrFET with $V_{th} = -0.2$ V. Thus, when the driver is working in the linear region with unit receptivity, the load is in its saturation region. The supply voltage $V_{DD} = 1$ V in both cases.

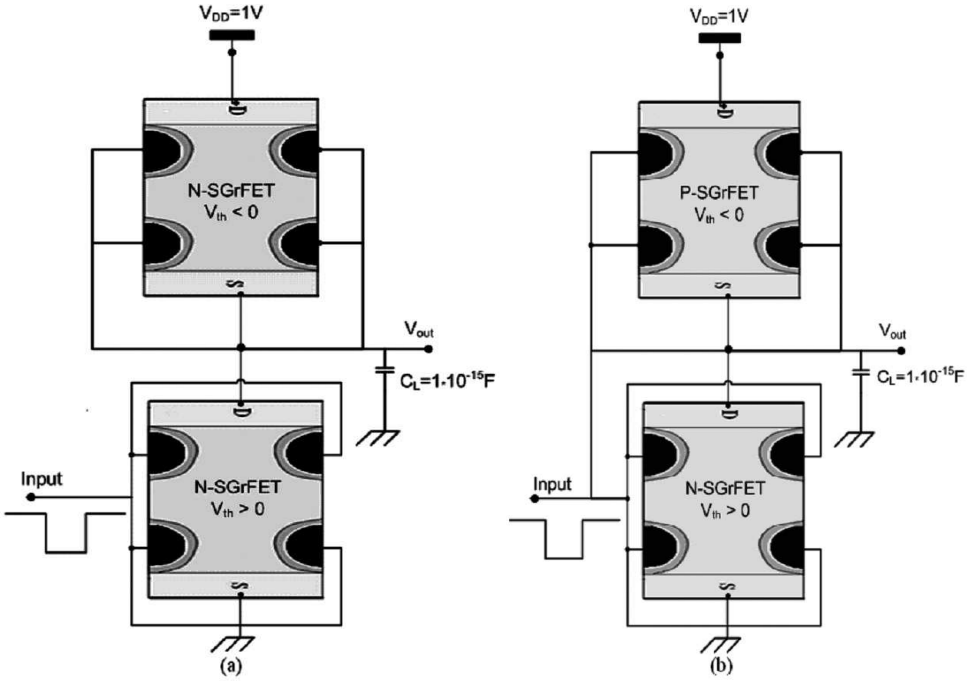

Fig. 3. (a) n-SGrFET inverter, (b) C-SGrFET inverter.

Both inverter circuits are given in Fig. 3. The value of the capacitive load, C_L in Fig. 3 is chosen as the input capacitance of the following SGrFET (its value can be changed to accommodate the fan-out of a specific circuit). To estimate C_L we compose the oxide capacitances of the 4 half gate cylinders (this result is close to that extracted from AC simulations):

$$C_L = 2\varepsilon_{ox}\varepsilon_o \frac{(2\pi r_{in})}{t_{ox}} h \tag{2}$$

Where ε_{ox} is the permittivity of the oxide; ε_0 is the permittivity of vacuum;h is the thickness of the Si channel; t_{ox} is the gate oxide thickness and r_{in} is the inner radius of the gate cylinder.

Figure 4 shows the DC transfer characteristics of both inverter circuits.

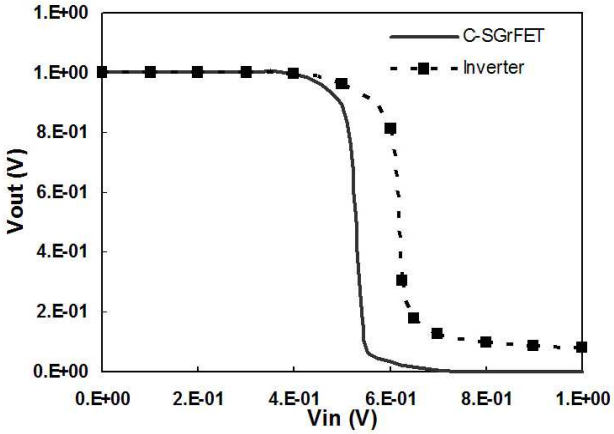

Fig. 4. Comparison of the transfer characteristics of the n-SGrFET (dashed line) and C-SGrFET (full line) inverter.

The C-SGrFET provides better performance than the n-SGrFET inverter, similar to other CMOS technologies. Power consumed in the C-SGrFET circuit is also lower because current is only drawn when switching [3] whilst for the n-SGrFET inverter a small current is flowing for high input voltages on the gate. The rise time (t_r) is defined as the time taken for the output voltage to go from 10% to 90% of its final value, t_r=18.6 ps related to n-SGrFET inverter. This is due to the faster switching speed of n-SGrFET device as a load in n-SGrFET inverter circuit configuration than p-SGrFET in C-SGrFET circuit configuration when input is going from L to H value.The noise margins (NM) of both types of inverters are extracted following the standard procedure [5]. There are two different noise margins, one for H (1V) and one for L (-0.3V). These NMs are given by [4] (we use the same notation as in [4]):

$NM_H = V_{OH} - V_{IH}$

$NM_L = V_{IL} - V_{OL}$.

The results are summarized in Table 3.

Table 3. Noise Margin and ON-OFF region for both n- and C-SGrFET inverter (see resp. Fig. 3a & Fig. 3b)

Inverter	V_{OL} [V]	V_{OH} [V]	V_{IL} [V]	V_{IH} [V]	NM_L [V]	NM_H [V]
Fig. 3a	0.15	0.92	0.55	0.67	0.4	0.25
Fig. 3b	0.06	0.95	0.47	0.57	0.31	0.38

3.2. NAND Logic

One of the key features in SGrFETs is its multi-gate functionality. A two-device NAND (Fig. 5 (a)) can be generated using the split-gate character presented in section II. Figure 5 (b) shows the transient analysis of the NAND logic.

The NAND circuit with the SGrFET has the same circuit configuration as the n-SGrFET inverter (Fig. 3a). In Fig. 4 one can see that the n-SGrFET inverter

does not switch completely off when the input goes high. Increasing the width of the enhancement mode n-FET ameliorates the problem but is not sufficient to solve it (this will be illustrated with the XOR example). The SGrFET device structure, however, offers the possibility to solve this problem by adding extra unit cells to the driver. This increases current drive whilst retaining the other FET parameters. The circuit of Fig. 5(a) shows a 3 unit cell driver. Using this approach the circuit switches completely off when the input is high as shown in Fig. 5(b). Note that the total channel width of the SGrFET driver with 3 unit cells is $3xW_U$ with W_U the width of one unit cell.

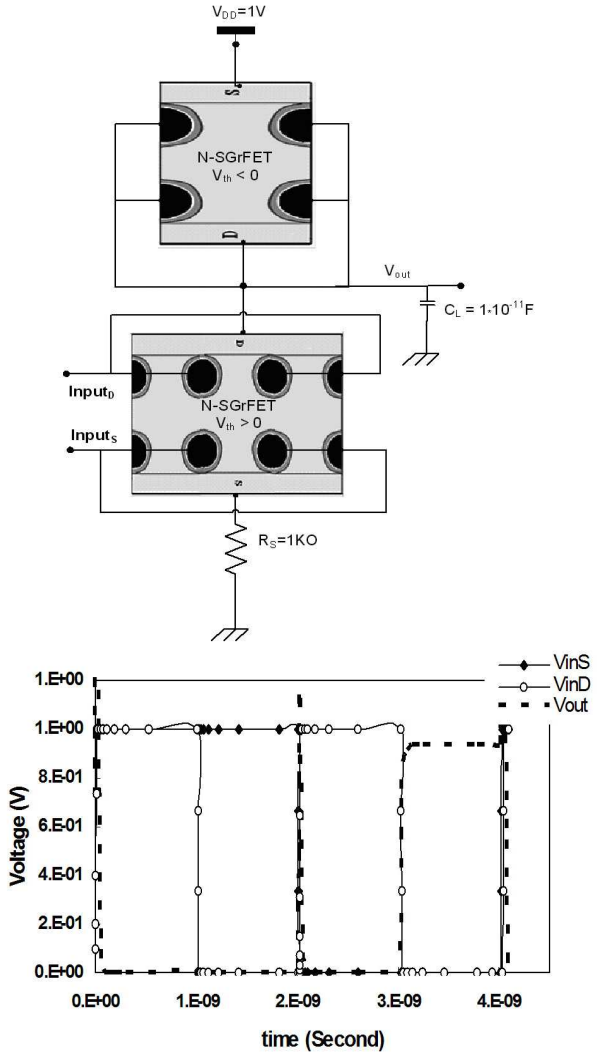

Fig. 5. (a) Schematic circuit of a SGrFET NAND; (b) NAND Output/Inputs Voltages vs. time. VinS is the gate voltage on row 1 and VinD is the gate voltage on row 2.

3.3. NOR Logic

NOR logic is presented also using two devices, an n-SGrFET as follower and a p-SGrFET as driver. Figure 6 shows the schematic circuit and transient response. In the NOR operation the p-SGrFET driver takes the split-gate function, whilst the n-SGrFET load functions in single gate contact mode. The p-type device is working in enhancement mode and the n-type in depletion mode. As shown in Fig. 6(a), as in the NAND logic, the driver is comprised of three unit cells.

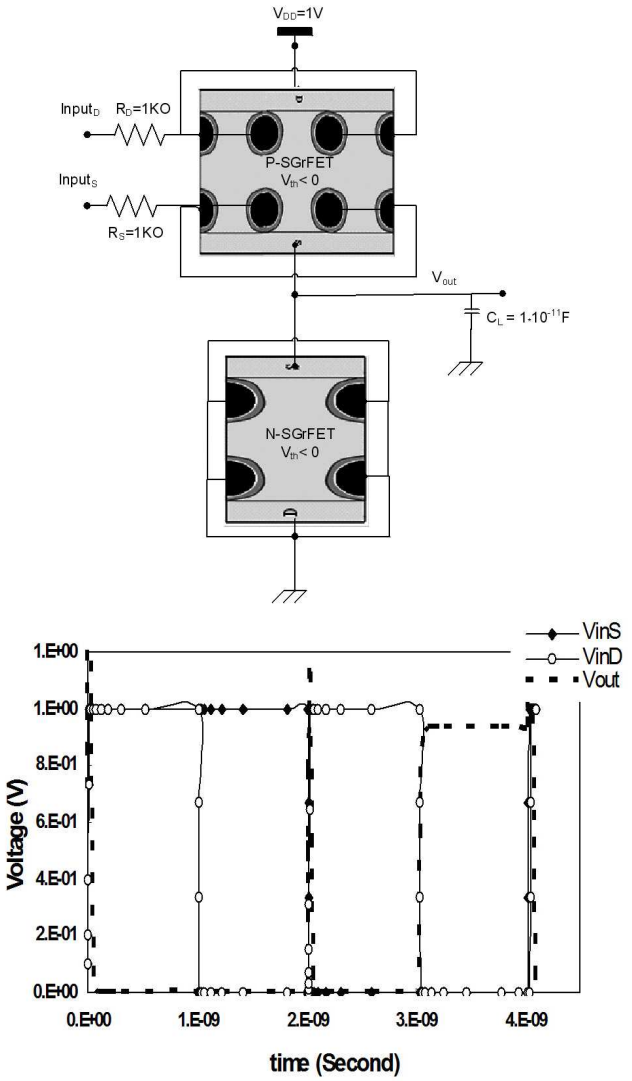

Fig. 6. (a) Schematic circuit of a SGrFET NOR;
(b) NOR Output/Inputs Voltages vs. time.

3.4. XOR Logic

An XOR circuit can also be constructed with only two SGrFETs. We present two different ways to implement the SGrFET XOR circuit. One approach will use an increased width for the n-channel driver via an increase in L_c. The other approach will use the increase in the number of unit cells used in the driver as done in the previous two circuits. Figures 7 and 8 give respectively an XOR with a single and triple unit cell driver.

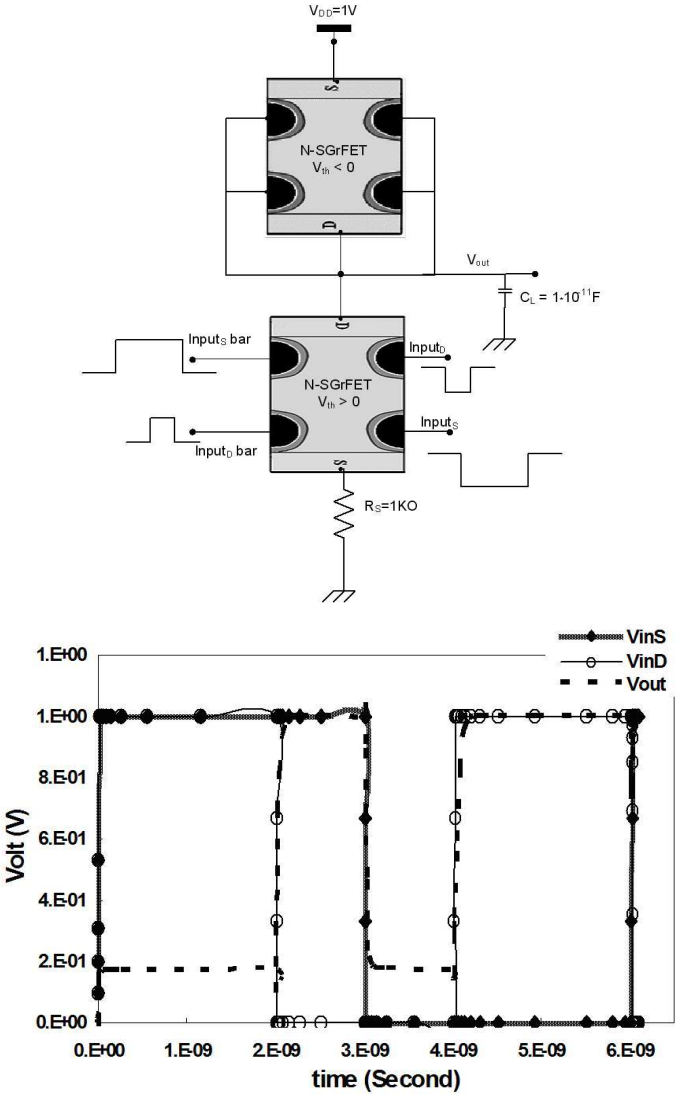

Fig. 7. (a) Schematic circuit of a SGrFET XOR;
(b) XOR Output/Inputs Voltages vs. time.

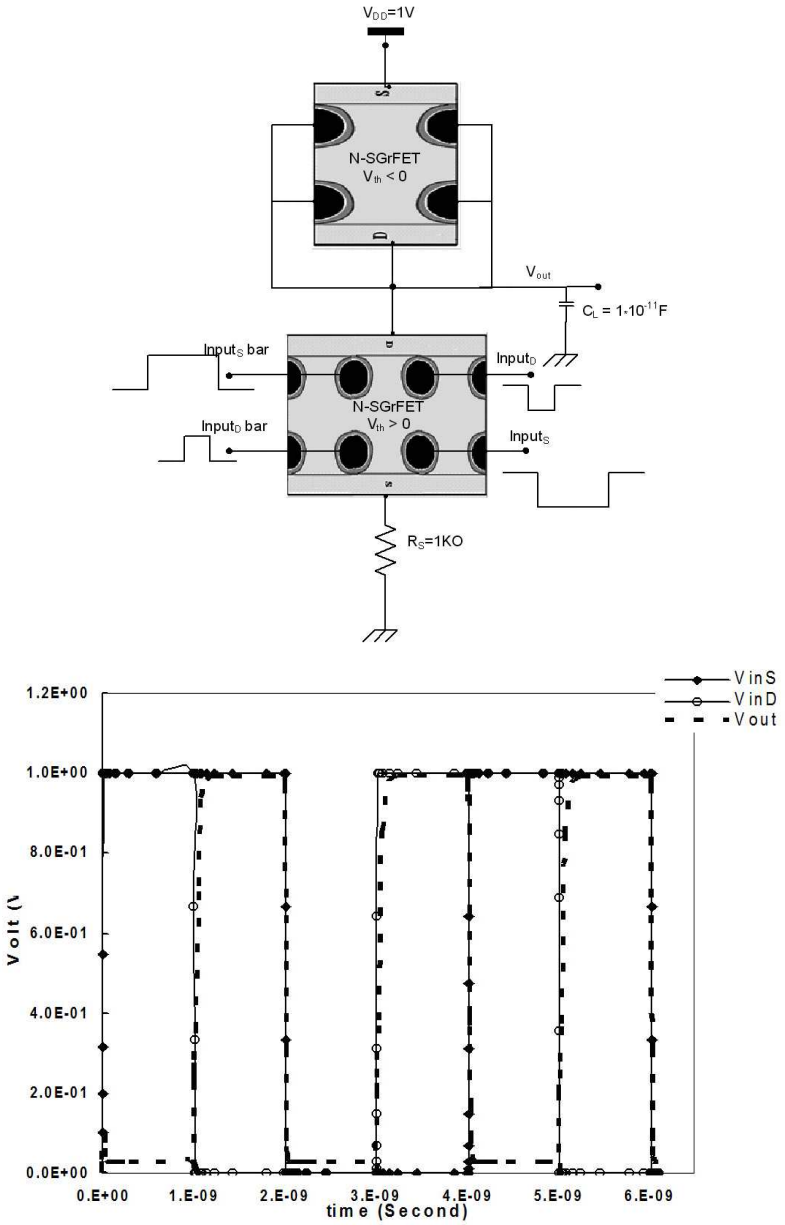

Fig. 8. (a) Schematic circuit of a SGrFET XOR with triple unit cell driver; (b) XOR Output/Inputs Voltages vs. time.

The XOR with the one unit cell driver uses the width relationship:
$L_{c-driver}/L_{c-load} = 2$
Thus the distance between the gate cylinders in one row (channel) increases. As long as this distance remains within two times the maximum depletion width range,

the control of the channel by the gates is diminished but not impeded. This approach results in a 0.2V OFF output voltage (see Fig. 7 (b)). If L_c is increased further then the output does not turn ON completely when the input is low. In general, increasing L_c whilst maintaining the other geometrical parameters constant is unadvisable because of a reduced gate control for increasing L_c. The width of the structure can also be increased by increasing the gate cylinder diameter. This would not have deteriorated the gate control to the same amount and would also have increased the current drive. Better however is increasing the number of unit cells whilst keeping all other geometrical parameters constant. This is illustrated in Figure 8.

The output of the XOR with the 3-unit-cell driver switches completely off as can be seen from Fig. 8(b).

The total width of the driver of Fig. 7 is:

$$W_{tot} = 2 \times t_{ox} + L_O + L_c = 154 \text{ nm}$$

The total width of the driver in Fig. 8 is:

$$W_{tot} = 3 \times W_U = 3 \times 104 \text{ nm} = 312 \text{ nm}$$

Thus the complete switch-OFF character comes at a price of increased footprint. Note that increased current drive can also be achieved by increasing the Si body thickness. However this analysis is beyond the scope of this 2D analysis.

4. Conclusion

We presented the simulated DC and transient performance of the SGrFET with independent double gate for digital applications. First the SGrFET was used in a classical circuit configuration with connected gate fingers and the transient performance of C-SGrFET and EDMOS inverter was presented. The results demonstrate the superior performance of the complementary approach with ps switching times and 0.4 V maximum noise margin.

In the second part of the paper the multi-functionality offered by the SGrFET in the independent double gate configuration was exploited in three logic circuits: NAND, NOR and XOR, which can all be realized using only two SGrFETs. Switching times are of the order of ps. It was demonstrated that the OFF state in the logic circuits can be improved by using a SGrFET driver with an appropriate number of unit cells rather than increasing the width of the unit cell itself. For the SGrFET a multi-unit cell approach is not more complicated from a device fabrication point of view than a single unit cell approach.

These simulation results demonstrate the potential advantage of using a SGrFET for logic applications.

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