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Streamlined Design of SiGe Based Power Amplifiers

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Abstract. This paper presents a streamlined design flow for an integrated power amplifier. For a given set of amplifier specifications and BiCMOS process parameters, a software routine computes passive component values for a Class-E or Class-F based power amplifier. The routine includes a matching network for standard impedance loads. Spiral inductor search algorithm is used to generate inductors with Q-factors optimised at a desired frequency. Operation of the software routine is demonstrated by simulations in Austriamicrosystems 0.35 μm single-supply process for the 10 dBm, 2.4 GHz power amplifier design.

Key words: BiCMOS process, spiral inductor, Class-E amplifier, Class-F amplifier, impedance matching, SPICE netlist.

1. Introduction

The power amplifier (PA) technology has become highly integrated into several process technologies including SiGe BiCMOS [1]. Original PA designs were based around metal-oxide semiconductor (MOS) transistors, but after the introduction of a bipolar transistor with a wide-gap emitter, or HBT, bipolar transistors emerged as the preferred choice because of their higher gain and current densities at radio frequencies (RF). The SiGe BiCMOS process offers both MOS transistors and HBTs, making it an excellent choice for inexpensive PA integration.

In this paper, a new design methodology for rapid design of BiCMOS Class-E and Class-F PAs [2] is proposed. For a given set of specifications, such as the PA bandwidth, centre frequency and class of operation, this methodology is used to design an optimal PA and to export its SPICE netlist. The method is coined as a software routine. The same routine determines geometry of the spiral inductor that gives an optimised quality factor, using process parameters for a particular BiCMOS process. Extracted layout of the inductors can be imported into the layout design software for the correct layout-level modelling, thus overcoming one of the major drawbacks of the spiral inductor design. To verify this software routine, a Class-E PA and a Class-F PA have been designed and simulated in the SiGe S35 (0.35 µm BiCMOS) process from Austriamicrosystems (AMS).

2. Theory

Both Class-E and Class-F amplifiers are switching type PAs and exhibit theoretical efficiencies of 100%.

2.1. Class-E PA

The Class-E amplifier uses combination of a series resonator and shunt capacitor to shape the collector voltage and current waveforms in order to deliver maximum power to the load. Fig. 1 shows a single ended Class-E PA [3]. Simplified analysis of the PA can be performed if it is assumed that L_1performs as an RF choke (RFC), output capacitance of the transistor is independent of the switching voltage and it can be included in C_1, and transistor is an ideal switch with zero resistance and zero switching time, open for half of the signal period. From [3], the value of the optimum load resistance to deliver the highest power to the load $P_{\text{out max}}$ with peak voltage (v_{peak}) equal to supply voltage V_{CC} is

$$R_L = \frac{2}{\frac{\pi^2}{4}+1} \cdot \frac{V_{CC}^2}{P_{\text{out max}}} \tag{1}$$

The passives L_2, C_1 and C_2 are calculated if the loaded Q-factor of the resonant tank (Q_L) and resonant frequency (f_0) are known:

$$L_2 = \frac{Q_L R_L}{2\pi f_0}, \tag{2}$$

$$C_1 = \frac{1}{2\pi f_0 R_L \left(\frac{\pi^2}{4}+1\right)\frac{\pi}{2}}, \tag{3}$$

and

$$C_2 = \frac{1}{(2\pi f_0)^2 L_2} \cdot \left(1 + \frac{1.42}{Q_L - 2.08}\right). \tag{4}$$

Minimum required inductance for L_1 to act as an RFC is given by [4]:

$$L_{1\,\min} = \frac{5}{8}(\pi^2 + 4)\frac{R_L}{f_0}. \tag{5}$$

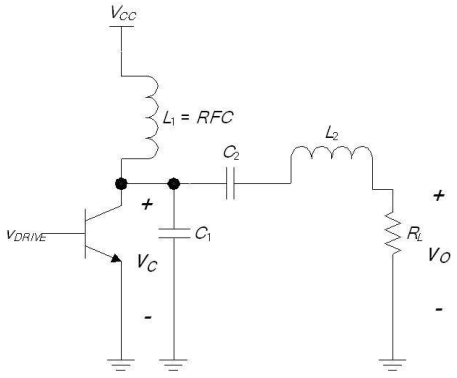

Fig. 1. Class-E PA circuit schematic.

2.2. Class-F PA

The Class-F amplifier includes the waveform-shaping circuitry in its output network which shapes collector waveforms in such a way that load appears to be short at even harmonics and open at odd harmonics. As a result, the ideal collector voltage waveform approximates a square wave, while the collector current waveform approximates a half-sine wave. At low gigahertz frequencies, passive resonators are used for waveform shaping. Ideal Class-F amplifiers would require an infinite number of resonators to correctly shape the output waveforms, but most monolithic integrated Class-F amplifier implementations consider only a few harmonics, usually two or three. Figure 2 shows the Class-F PA with resonators up to the fifth harmonic [5]. In this circuit, a tank at $3f_0$ provides an open circuit at $3f_0$ and short circuit at $2f_0$, whilst the tank at $5f_0$ provides an open circuit at $5f_0$ and short circuit at $4f_0$. With sufficiently large RFC, the theoretical efficiency of the circuit is 90.5% [6].

The design is performed for the optimum load resistance:

$$R_L = \frac{\gamma_V^2 V_{CC}^2}{2P_{\text{out max}}}. \tag{6}$$

DC current needed for correct waveform shaping is given by:

$$I_{DC} = \frac{\gamma_V V_{CC}}{\gamma_I R_L}. \tag{7}$$

Peaks of the collector voltage and current waveforms are given by:

$$v_{Cm} = \delta_V V_{CC}, \tag{8}$$

and

$$i_{Cm} = \delta_I I_{DC}. \tag{9}$$

Coefficients γ_V, γ_I, δ_V and δ_I are the maximum efficiency coefficients defined in Table 1 [6].

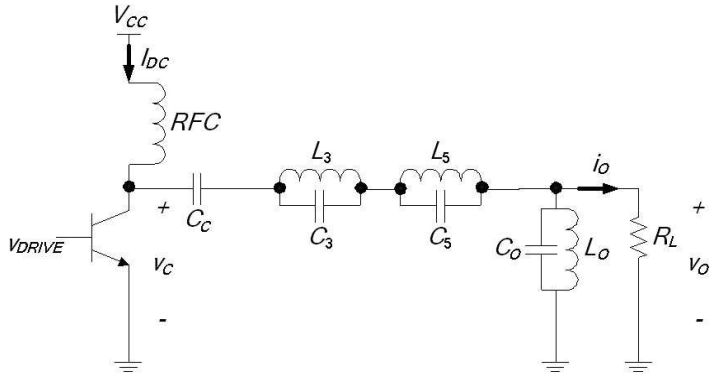

Fig. 2. Class-F PA circuit with resonators up to the fifth harmonic.

Table 1. Maximum-efficiency waveforms coefficients

Coefficient	Value (resonators up to 5^{th} harmonic)
γ_V	1.2071
δ_V	2
γ_I	1.5
δ_I	3

2.3. Spiral Inductor

Spiral inductors are used to implement all inductors for the PA. A die photograph of an example of a spiral inductor is shown in Fig. 3. A lumped single-π nine-component inductor model shown in Fig. 4 is sufficient to accurately model spiral inductors for frequencies below resonance [7]. This topology correctly models parasitic effects of the metal spiral (C_S and R_S) and oxide below the spiral (C_{ox}), as well as the substrate effects (C_{Si} and R_{Si}), but does not model the distributive capacitive effects. L_S is inductance at a given frequency, calculated by the data-fitted monomial expression that results in an error typically not greater than 3% [7]. Inductance in nanohenries (nH) is calculated as:

$$L_S = \beta d_{\text{out}}^{\alpha_1} w^{\alpha_2} d_{\text{avg}}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}, \tag{10}$$

where $\beta = 1.62{\cdot}10^{-3}$, $\alpha_1 = -1.21$, $\alpha_2 = -0.147$, $\alpha_3 = 2.40$, $\alpha_4 = 1.78$ and $\alpha_5 = -0.030$, are the coefficients for square geometry and d_{out}, d_{in}, n and s are the outer diameter of the spiral, inner diameter of the spiral, the number of turns and turn spacing respectively. Although the inductance itself is independent of frequency, parasitics add to the apparent value of inductance.

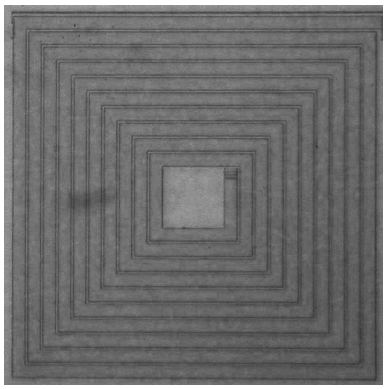

Fig. 3. The photograph of a spiral inductor.

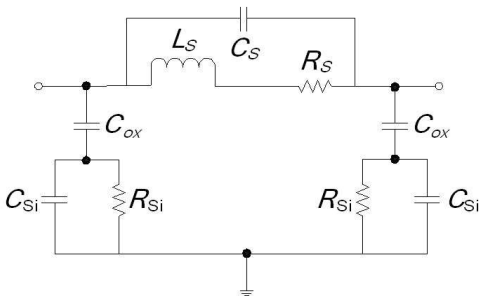

Fig. 4. Nine-component spiral inductor model [7].

Apart from inductance, inductors are also commonly characterized by means of the Q-factor. For a single-π model, the inductor Q-factor can be calculated as [8]

$$Q = \frac{\omega L_S}{R_S} \cdot \frac{R_P}{R_P + \left[\left(\frac{\omega L_S}{R_S}\right)^2 + 1\right] R_S} \cdot \left[1 - (C_P + C_S) \cdot \left(\omega^2 L_S + \frac{R_S^2}{L_S}\right)\right], \quad (11)$$

where

$$R_P = \frac{1}{(2\pi f_0)^2 C_{ox}^2 R_{\mathrm{Si}}} + \frac{R_{\mathrm{Si}} \left(C_{ox} + C_{\mathrm{Si}}\right)^2}{C_{ox}^2}, \quad (12)$$

and

$$C_P = C_{ox} \cdot \frac{1 + (2\pi f_0)^2 \left(C_{ox} + C_{\mathrm{Si}}\right) C_{\mathrm{Si}} R_{\mathrm{Si}}^2}{1 + (2\pi f_0)^2 \left(C_{ox} + C_{\mathrm{Si}}\right)^2 R_{\mathrm{Si}}^2}. \quad (13)$$

Low Q-factors of spiral inductors are attributed to the losses of the inductor spiral, substrate loss in the semiconducting silicon substrate and self resonance loss due to the total capacitance, $C_P + C_S$.

3. Software Routine

Class-E and Class-F PAs as well as inductor design equations were used to develop a software routine for the PA design.

At the beginning of the execution of the routine a user is required to enter design parameters for the Class-E or Class-F PA design. These include operating frequency, voltage supply and required output power, as well as some PA class-specific parameters. After all necessary PA components are computed, the user has a choice to perform output impedance matching to the standard impedance of 50 Ω. The routine employs impedance matching which uses discrete components. Three impedance networks are available: a wideband two-component network (L network) and two narrowband three-component networks (T and Π networks). The user can also choose to invoke the inductor search algorithm, shown in Fig. 5, to design spiral inductors for all inductors required for the full PA design, including matching inductors.

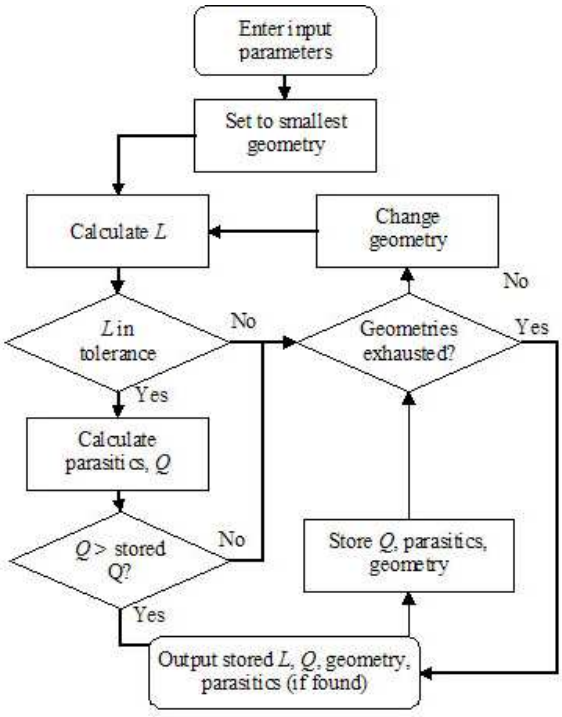

Fig. 5. Spiral inductor search algorithm.

The intention behind this algorithm is to find a square inductor geometry resulting in the highest Q-factor for the specified inductance given some design constraints. The process parameters required for the routine can either be specified on a separate screen, or they can be imported from a process configuration file. For the AMS BiCMOS process, the process parameters for both 3-metal and thick-metal inductors are included as program defaults. Furthermore, the program can also export SPICE

netlist of each inductor structure, complete with the inductance value and parasitics, and a GDS file, which contains the mask geometry information of any inductor [9]. The netlist extraction is also possible for the complete PA implementation. These netlists can be used in SPICE simulations to avoid drawing schematics. The GDS file can be imported into the layout software to eliminate the need for manual drawing of inductor layout structures.

4. Results

One Class-E and one Class-F PA were designed using the software described previously in the AMS S35 process for 2.4 GHz ISM band and aimed power of 10 dBm. Because of the nonideal properties of the driving transistor, the actual design was performed for a higher output power. The schematics of the two configurations including the output matching networks are shown in Fig. 6 and Fig. 7. Table 2 lists the input and calculated values of all required Class-E PA quantities. Table 3 lists the same information for the Class-F PA design.

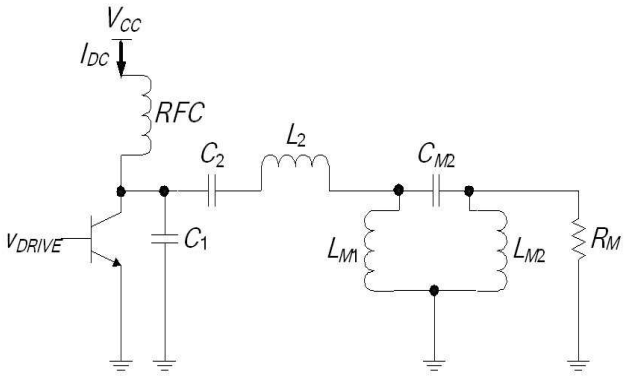

Fig. 6. Final circuit diagram of Class-E PA.

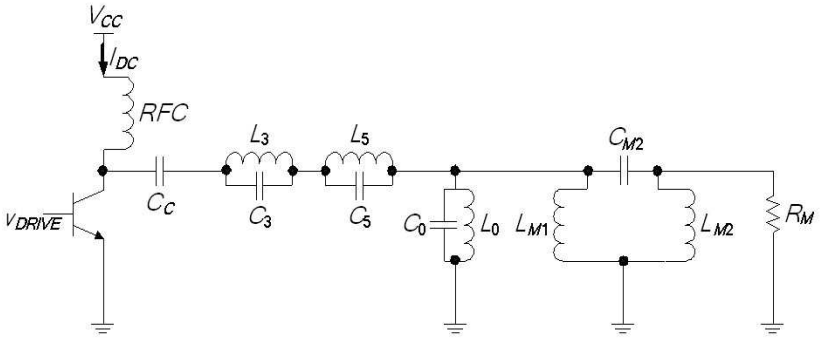

Fig. 7. Final circuit diagram of Class-F PA.

Table 2. Input and computed parameters for Class-E PA

Parameter	Value	Unit	Parameter	Value	Unit
V_{CC}	1	V	Q_L	5	–
Matching	Π ICI*	–	$P_{\text{out max}}$	17	dBm
R_L	11.5	Ω	I_{DC}	50	mA
C_2	1.71	pF	L_{M1}	1.02	nH
L_2	3.83	nH	C_{M1}	2.85	pF
C_1	1.05	pF	L_{M2}	1.38	nH
V_{BIAS}	0.82	V	R_M	50	Ω

*Inductor-capacitor-inductor

Table 3. Input and computed parameters for Class-E PA

Parameter	Value	Unit	Parameter	Value	Unit
V_{CC}	1.5	V	#resonators	5	–
Matching	Π ICI*	–	$P_{\text{out max}}$	11	dBm
R_L	50	Ω	C_3	0.98	pF
L_0	1	nH	L_5	0.5	nH
C_0	4.4	pF	C_5	0.36	fF
L_3	0.5	nH	I_{DC}	16.6	mA
V_{BIAS}	0.8	V	R_M	50	Ω

*Inductor-capacitor-inductor

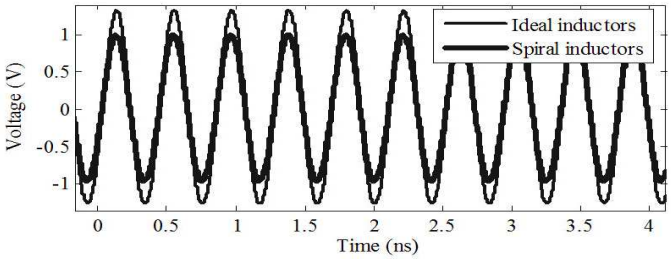

Fig. 8. Output voltage waveforms for Class-E PA with ideal inductors (thin line) and spiral inductors (thick line).

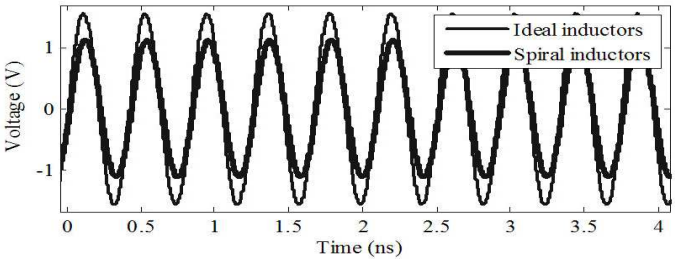

Fig. 9. Output voltage waveform for Class-F PA with ideal inductors (thin line) and spiral inductors (thick line).

Output waveforms (v_0) of two simulated systems are shown in Fig. 8 and Fig. 9, respectively. In both cases, waveforms are shown for designs using ideal inductors as well as spiral inductors implemented in thick-metal process. Furthermore, it has been assumed that the 100 nH RFC inductors for both designs were external to the integrated circuit (IC).

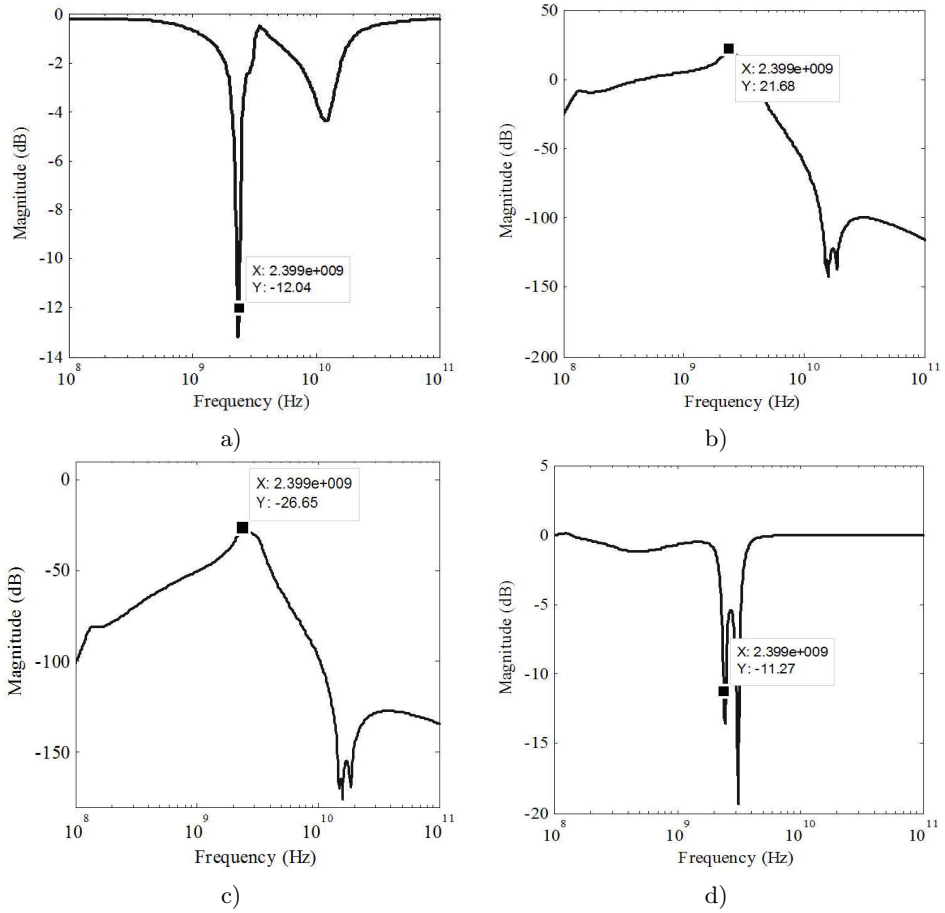

Fig. 10. Magnitudes of (a) Input port voltage reflection coefficient (S_{11}), (b) Forward voltage gain (S_{21}), (c) Reverse voltage gain (S_{12}) and (d) Output port voltage reflection coefficient (S_{22}) of the designed Class-E PA system.

For the design with ideal inductors, the output voltage waveform has a power of about 12.1 dBm and 13.9 dBm for the Class-E and Class-F design respectively, higher than the design specification. When transistor biasing and spiral inductors were included, the amplifiers assumed the output power of about 9.6 dBm and 10.9 dBm, approximately meeting the proposed design specification. The decrease of 2.5 dBm (Class-E design) or 3 dBm (Class-F design) was expected and it could be attributed to the presence of parasitics in inductors. Collector efficiencies of the Class-E stage

were 41.3% for an ideal design and 23.5% for the practical design. For the Class-F stage, efficiencies were 51% for ideal design and 20% for the practical design. Finally, the S-parameters after input matching was performed for the two amplifiers are shown in Fig. 10 and Fig. 11, which proves the correct operation of designed PAs.

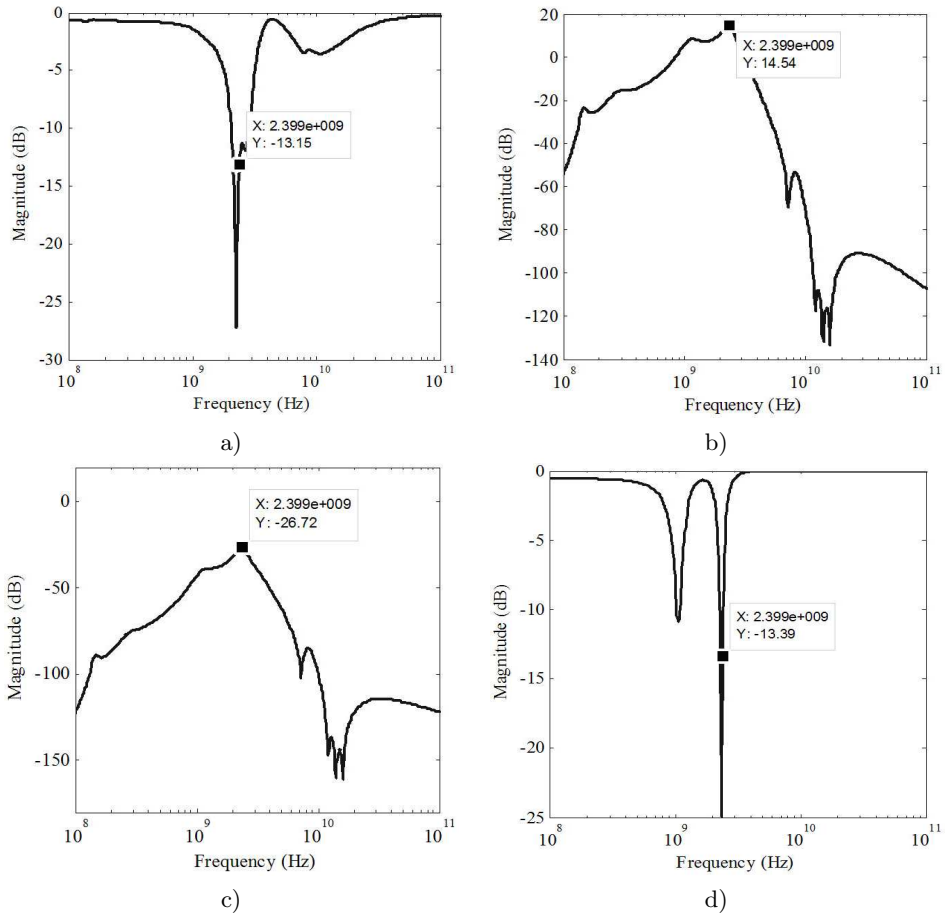

Fig. 11. Magnitudes of (a) Input port voltage reflection coefficient (S_{11}), (b) Forward voltage gain (S_{21}), (c) Reverse voltage gain (S_{12}) and (d) Output port voltage reflection coefficient (S_{22}) of the designed Class-F PA system.

5. Conclusion

In this paper, a software routine for the design of the SiGe BiCMOS PAs was presented. Apart from determining optimum values of passives needed for correct waveform filtering for the Class-E and Class-F PAs, the routine handles output impedance matching and spiral inductor design, as well as SPICE netlist and layout extrac-

tion. The streamlined use of the software-aided design described in this paper was demonstrated by designing and simulating two complete 2.4 GHz PAs.

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