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Design Trade-offs and Limitations of a LC-Ladder and Capacitive Feedback LNA and its Application at mm-Wave Frequencies

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Abstract. Simulation results of a LC-ladder and capacitive feedback low noise amplifier over the 60 GHz unlicensed band is presented. A gain of 14.2 dB was obtained with S_{11} less than –15 dB and a noise figure of 5.2 dB. These results deviate significantly from theory however and as such possible explanations for these deviations are presented as well as a suggestion for the improvement of the mathematical model. Other design trade-offs present in very wideband designs at lower frequencies are also quantified and equations for the maximum corner frequency and bandwidth as a function of noise figure are derived.

Key words: low noise amplifier; mm-wave; LC-ladder filter; capacitive feedback; frequency limitations; performance trade-offs.

1. Introduction

In today's market there is an ever growing high-bandwidth, low-power and low-cost wireless networking demand. A variety of high-bandwidth wireless technologies such as Ultra-wideband (UWB) and WiMAX have been proposed to take advantage

of this extremely large and varied applications space. Subsequently a number of wideband low noise amplifier (LNA) configurations achieving good specifications have been proposed [1], [2], [3].

These wideband schemes have however often failed to deliver since they are reliant on extensive baseband processing which quickly becomes complex and consume large amounts of power [4]. In contrast there is an abundance of bandwidth available in the unlicensed part of the mm-wave frequency band (57–64 GHz), which can be leveraged against power consumption in mobile devices. In addition Silicon Germanium (SiGe) technology has offered a low cost alternative to the more traditional III-V compounds making mm-wave radios a very attractive prospect.

Mm-Wave LNAs are usually implemented as narrow band amplifiers using active devices characterised by S-parameters and tuned by distributed passive structures, however a RF analogue approach combining lumped passive devices with the transistor model to achieve the desired functionality can also be used [5]. The question of whether wideband LNA design techniques based on the latter approach can also be used to achieve good results in the mm-wave range is investigated in this paper.

The capacitive shunt-shunt feedback LNA configuration with LC-ladder network, shown in Fig. 1, can theoretically achieve an arbitrary bandwidth due to the LC-ladder network providing a wide matched bandwidth [3]. It is thus reasonable to assume that this also applies at mm-wave frequencies; however simulation results of designs for operation beyond 20 GHz prove that performance deviates significantly from theory and proper matching is not obtained.

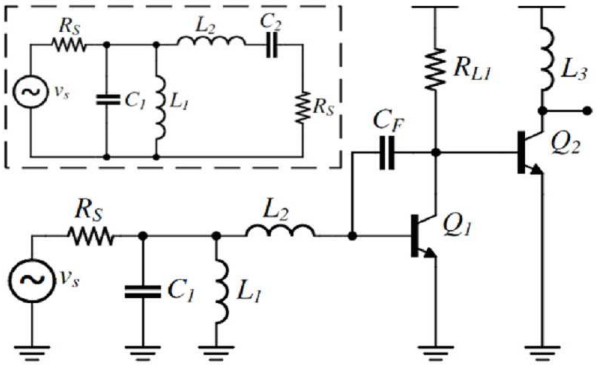

Fig. 1. Schematic of the LC-ladder and capacitive shunt-shunt feedback amplifier [3] with the equivalent LC-ladder circuit [1].

When attempting to achieve very wide bandwidths using this configuration the noise figure (NF) and gain are also often not within acceptable limits.

Thus although this configuration can achieve good results over reasonable frequency bands up to 20 GHz [3], [6] there are some limitations to the specifications that can be achieved and as such it is desirable to quantify the limits of this configuration in order to discern when it would be the optimal choice for a given implementation.

In the following sections a 60 GHz implementation is discussed and the frequency limitations are subsequently quantified, as well as equations derived to determine the

absolute maximum frequency of operation and subsequent maximum bandwidth to achieve a given NF specification.

2. 60 GHz LNA design and simulation results

The design process in [3] was followed in an attempt to use the LC-ladder and capacitive feedback configuration over the 60 GHz unlicensed band. The final design achieved 14.2 dB gain with 1.4 dB ripple, as well as S_{11} of less than –15 dB around the centre frequency. The results are shown in Fig. 2. A relatively high NF of 5.2 dB was obtained, but this is comparable to the results of other designs in literature as shown in Table 1. The IIP3 and 1 dB compression point are –8.4 dBm and –20 dBm respectively.

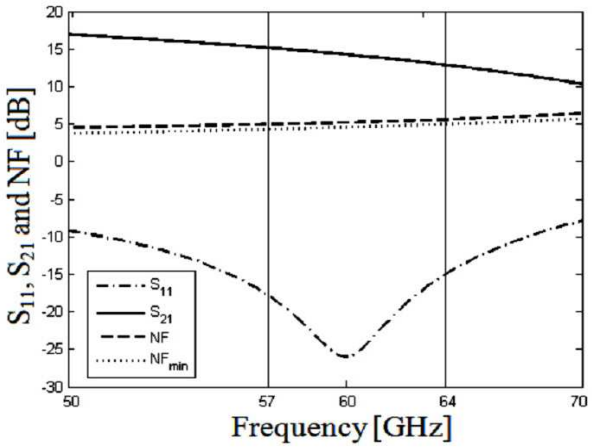

Fig. 2. Simulated results of the LC-ladder capacitive feedback LNA implementation at 60 GHz.

Table 1. Comparison of results to other state-of-the-art mm-wave LNAs

Ref.	Technology	f [GHz]	S_{11} [dB]	S_{21} [dB]	NF [dB]	IIP3 [dBm]	P_{1dB} [dBm]	P [mW]
This work	0.13 µm SiGe BiCMOS	60	< -15	14.2	5.2	–8.4	–20	25.5
[7]	90 nm CMOS	58	< -10	14.6	5.5	–6.8	–	24
[8]	0.13 µm SiGe BiCMOS	60	< -10	18	5	–	–	7.5
[9]	0.25 µm SiGe BiCMOS	60	< -10	18	6.7	–	–18	20
[10]	0.12 µm SiGe BiCMOS	58	< -10	14.8	4.1	–2	–12	8.1

The final input matching network component values are $C_1 = 92$ fF, $L_1 = 400$ pH and $L_2 = 116$ pH. The feedback capacitance (C_F) was removed and thus $C_{BC} = C_\mu$

which is the minimum value. A 1.5 V supply was used with collector currents $I_{C1} =$ 5 mA and $I_{C2} = 12$ mA. The first stage load resistance is 300 Ω and the second stage load inductance 540 pH.

These values are however not those obtained from the design equations but were derived iteratively from the initial values during the simulation and optimisation process.

3. Design Limitations

Based on the results obtained from the 60 GHz implementation of this configuration it is clear that at such high frequencies the analytical results no longer track simulation results sufficiently. This indicates that additional factors, other than those included in the initial analysis below 20 GHz, are present. The causes of these deviations and other limitations to high frequency operation are discussed next.

3.1. Transistor input impedance approximation

The series capacitance (C_2) and resistance of the LC-ladder network (refer to Fig. 1) is synthesized using the capacitive feedback resulting in a Miller impedance of [2]:

$$Z_M = \frac{R_{L1}}{(1 + g_{m1}R_{L1})}\left(1 + \frac{C_{L1}}{C_{BC}}\right) + \frac{1}{j\omega\left(C_{\pi 1} + C_{BC}\left(1 + g_{m1}R_{L1}\right)\right)}, \tag{1}$$

when $1 + g_{m1}R_{L1} \ll j\omega R_{L1}C_{L1}$, where R_{L1}, C_{L1} and g_{m1} are respectively the first stage load resistance, load capacitance and transconductance, and $C_{BC} = C_{\mu 1} + C_F$.

When the assumption no longer holds at high frequencies the $j\omega R_{L1}C_{L1}$ term is included in the equation for the Miller impedance and it can instead be written as:

$$Z_M = \frac{R_{L1}}{(1 + j\omega R_{L1}C_{L1} + g_{m1}R_{L1})} + \frac{1}{j\omega\left(C_{\pi 1} + C_{BC}\left(1 + \dfrac{g_{m1}R_{L1}}{1 + j\omega R_{L1}C_{L1}}\right)\right)}. \tag{2}$$

Thus it is seen from (2) that in such a case C_2 will decrease with frequency as the voltage gain decreases, and the equivalent resistance also becomes frequency dependent and will only appear resistive over a limited frequency band.

3.2. Transistor gain limitation

Typical SiGe transistors have unity gain frequencies of 200 GHz and therefore a typical first stage DC voltage gain of 10 (20 dB) results in a pole at 20 GHz.

Either this limit to the transistor gain or the output pole of the first stage given by [3]:

$$\omega_{P1} = \frac{1}{R_{L1}\left(C_{BC} + C_{L1}\right)} \tag{3}$$

results in a gain roll-off at –20 dB/decade above the corner frequency.

The design attempts to compensate for this roll-off through the inductive load of the second stage which introduces a zero in the overall frequency response and thus, ideally, results in a flat voltage gain at the output. However the second stage also has a finite f_T and as such cannot maintain a transfer function rising at +20 dB/decade at very high frequencies.

If more than one of these poles are within the frequency band of interest, as is often the case above 20 GHz, the overall voltage gain will no longer have a flat frequency response. Therefore the gain bandwidth product remains a fundamental limit to the bandwidth that can be achieved while maintaining reasonable gain per stage.

3.3. On-chip passive components

The most fundamental limit to the achievable frequency range is the available passive component values in a given transistor process, since all matching network components scale with inverse proportionality to frequency [3].

The upper corner frequency is determined by L_2 and C_1 and as such is limited by the minimum inductance and capacitance that are available. It would be possible to use parallel connected inductors to decrease the effective inductance; however this would consume a large chip area and also introduce additional large parasitic components into the circuit. The use of series connected capacitors to achieve smaller effective capacitance is more feasible, however C_1 is usually implemented as the pad capacitance and as such the use of another series capacitor is invalid.

The lower corner frequency is limited by the maximum inductance value that is available for L_1. Although C_2 also influences the lower corner the limitation on C_2 is usually due to the increased high frequency NF as discussed in Section 5.1 and not due to passive component limitations. Since the latter is usually the dominant limitation the maximum available L_1 is not significant.

3.4. Base- and collector current noise correlation

Collector current shot noise is not introduced at the base-collector junction as often assumed but in fact originates from the base-emitter junction where majority carrier electrons (in *npn* transistors) from the emitter cross the junction into the base. These noisy electrons are transported across the base to the base-collector junction during a time τ_n, which is the base transit time, resulting in correlation between the base- and collector current shot noise. According to the transport shot noise model these noise power spectral densities are given by [11]:

$$\overline{i_c^2} = 2qI_C, \tag{4}$$

$$\overline{i_b^2} = \overline{i_e^2} + \overline{i_c^2} - 2Re\left\{\overline{i_e i_c^*}\right\} = \left[2qI_B + 4qI_C\left(1 - Re\left\{e^{j\omega\tau_n}\right\}\right)\right], \tag{5}$$

$$\overline{i_b^* i_c} = \left\{\overline{i_e i_c^*}\right\}^* - \overline{i_c^2} = 2qI_C\left(e^{-j\omega\tau_n} - 1\right). \tag{6}$$

In the derivation of the equation for NF in [3] this correlation between the base- and collector current shot noise is neglected. This is similar to assuming the collector current shot noise is generated at the base-collector junction by setting $\tau_n = 0$, resulting in the conventional SPICE noise model. Although this approximation is feasible when $\omega \ll 1/\tau_n$, at 60 GHz which is much closer to the device f_T the noise correlation becomes non-negligible and the mathematical model of [3] overestimates the NF of the LNA.

4. Input matching modelling improvement

As discussed in Section 3.1, the approximation used in the derivation of the Miller impedance leads to inaccurate results at high frequencies. It can also be noted that the simple case of a constant load resistance and capacitance was used in the derivation of the transistor input impedance [2], [3], however the inductive load of the second stage in fact results in a second order equation for the load impedance.

The input impedance of the second stage is defined as:

$$Z_{IN,2} = R_{\pi 2} \left\| \frac{1}{j\omega C_{\pi 2}} \right\| Z_{M2}, \tag{7}$$

where Z_{M2} is the Miller impedance, and using the Miller theorem $Y_{IN,2}$ can be written as:

$$\begin{aligned} Y_{IN,2} &= \frac{1}{R_{\pi 2}} + j\omega \left[C_{\pi 2} + C_{\mu 2} \left(1 + j\omega L_3 g_{m2} \right) \right] = \\ &= \frac{1}{R_{\pi 2}} + j\omega \left(C_{\pi 2} + C_{\mu 2} \right) - \omega^2 g_{m2} L_3 C_{\mu 2}. \end{aligned} \tag{8}$$

Thus the load impedance of the first stage used in the Miller impedance calculation should rather be defined as the parallel combination of the first stage load resistance, the impedance of C_{L1}, and $Z_{IN,2}$.

The same small signal derivation can then be used to define the first stage input impedance more accurately by using this definition of Z_{L1} rather than a constant load resistance and capacitance, and this results in

$$Z_{T,IN} = \frac{Z_{L1} + \dfrac{1}{j\omega C_{BC}}}{1 + g_m Z_{L1}}. \tag{9}$$

The simple case is sufficient and convenient for the initial design, but the derivation of $Z_{T,IN}$ in (9) should be used when calculating the gain of the input matching network, as well as the load impedance Z_{L1} for determining the gain of the first stage. This will lead to the calculated results tracking simulation results more accurately.

5. Performance Trade-Offs

Apart from the physical constraints of the configuration affecting design at very high frequencies described in the previous section, certain performance trade-offs can also be observed at lower frequencies when very wideband designs are attempted.

5.1. Noise figure vs. Bandwidth

The complete equation for the NF of the amplifier was derived in [3]. However it was shown in [6] that the noise is dominated by the transistor voltage noise and as such the noise factor can be approximated as:

$$F \approx 1 + \left(\frac{1}{|Z_S|^2} + \left| 1 + \frac{Z_2}{Z_S} \right|^2 |\omega C_{BC}|^2 \right) \cdot R_S^2 \frac{\overline{v_{CE1}^2}}{\overline{v_{RS}^2}}, \tag{10}$$

where

$$R_S^2 \frac{\overline{v_{CE1}^2}}{\overline{v_{RS}^2}} = \left(r_b + \frac{V_T}{2I_{C1}} \right) R_S \tag{11}$$

and symbols are defined as in [3]. Noise increases sharply at high frequencies mainly due to the ωC_{BC} term. Thus for a given maximum NF specification operation up to a corner frequency ω_u is possible where ω_u can be increased by decreasing C_{BC}.

The value of C_{BC} is determined by the gain and the value of C_2, which is in turn determined by the lower cut-off frequency ω_l [3]. Thus, by substituting

$$C_{BC} \approx \frac{1}{\omega_l R_S \left(1 + g_{m1} R_{L1}\right)} \tag{12}$$

in (10) and after some manipulation the minimum lower cut-off frequency for a given maximum NF is derived as

$$\omega_l \approx \left[\frac{R_S \left(1 + g_m R_L\right)}{\omega} \sqrt{\left(\frac{\left(F_{\max} - 1\right)}{\left(r_b + \frac{V_T}{2I_C} \right) R_S} - \frac{1}{|Z_S|^2} \right) \div \left| 1 + \frac{Z_2}{Z_S} \right|^2} \right]^{-1} \Bigg|_{\omega = \omega_u} \tag{13}$$

where Z_S and Z_2 are also frequency dependent. Since ω_l is defined as a function of ω_u, (13) quantifies the bandwidth vs. NF limitation of this configuration.

Since a change in ω_l will result in a change in Z_S through L_1 and C_2 being modified, finding the correct solution for ω_l is iterative. Including the noise of the parasitic resistance of L_2, which also contributes somewhat at high frequencies, in the equation will provide even more accurate results.

5.2. Parasitic capacitance vs. Lower corner frequency

Since there is a minimum base-collector feedback capacitance, which is the parasitic C_μ of the transistor, it is apparent from (12) that there will be a maximum ω_l that can be achieved for a given first stage gain.

If C_2 is written in terms of ω_l, the maximum lower corner frequency is given by

$$\omega_{l\,\max} = \frac{1}{R_S\left(C_{\pi 1} + C_{\mu 1}\left(1 + g_{m1}R_{L1}\right)\right)}. \tag{14}$$

With capacitances of $C_{\pi 1} = 25$ fF and $C_{\mu 1} = 20$ fF typical of 0.13 µm processes, and a gain of 10 dB, the maximum lower corner frequency is approximately 30 GHz in a 50 Ω system.

By substituting ω_{lmax} and $C_{BC} = C_\mu$ in (13) and numerically solving for ω_u an associated maximum upper corner frequency can also be found.

It is possible to scale the transistor emitter length in order to reduce the parasitic capacitances of the transistor to make operation at higher frequencies more feasible; however the NF increases very rapidly with r_b since that is the dominating noise source in the system. Thus the NF vs. bandwidth trade-off remains as decreasing the emitter length to decrease capacitances will increase r_b.

6. Simulation Results

To verify (13) an arbitrary f_u of 18 GHz was chosen which is within the bound set by (14). The maximum allowable NF was chosen to be 4 dB and (13) including the noise from L_2 (which is subtracted from F_{max}) was then used to find $f_l = 2.5$ GHz which satisfies the NF requirement.

Using the design process in [3] the passive components and collector currents were calculated and the circuit was simulated using the IBM 8HP BiCMOS process design kits in Spectre. The simulated NF and S_{21} are shown in Fig. 3. S_{11} remains below –10 dB.

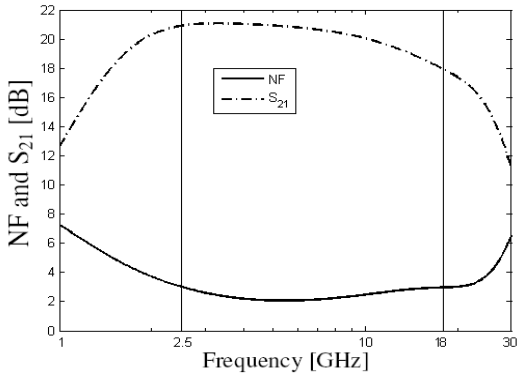

Fig. 3. Simulated NF and S_{21} results showing NF below 4 dB over the 2.5 GHz to 18 GHz band.

The NF is less than 4 dB over the frequency band of interest, indicating that (13) can be used to estimate the achievable bandwidth of the LNA configuration.

Since optimisation of the input matching network to minimise noise will reduce the NF at the upper cut-off frequency [6], f_l could be extended somewhat beyond this initial estimate.

7. Conclusion

The use of a lumped element design approach for wideband LNAs was investigated at mm-wave frequencies. Although results comparable to those in literature were obtained, the theory of the design process is no longer consistent with simulated results due to various second order effects present when operating close to the device f_T. It is therefore concluded that a distributed design approach is preferable for mm-wave design with current transistor technology.

The frequency limitations of the LC-ladder and capacitive feedback approach were discussed and equations for the NF vs. bandwidth trade-off were derived.

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