ROMANIAN JOURNAL OF INFORMATION SCIENCE AND TECHNOLOGY
Volume **13**, Number 3, 2010, 323–331

Discontinous-Time Comparator with State Saving

Valentin CHESARU[1], Cristian NEACŞU[1],
Claudius DAN[2], Mircea BODEA[2]

[1]O2Micro, Blvd. Vasile Milea no. 2F, Bucharest, Romania
E-mail: valentin.chesaru@o2micro.com,
cristian.neacsu@o2micro.com

[2] "POLITEHNICA" University of Bucharest, Romania
E-mail: claudius_dan@yahoo.com, mirceabodea@yahoo.com

Abstract. This paper presents the design of a low power discontinuous time comparator that saves its state in a digital latch circuit when entering shut-down mode. The designed low power comparator can be used in any integrated circuit to decrease power consumption in shut-down mode. The design is based on a simple and efficient idea: while the comparator is in shut-down mode, its previous state is stored in a latch. This idea can be easily applied to any "already designed" discontinuous – time comparator.

1. Introduction

Comparators are used today in every electronic circuit, due to their wide-spread applications and their well-known structure.

In the digital domain there are two major types of circuits – asynchronous and synchronous. Corresponding to these two categories the comparators can be classified in two categories: with continuous and discontinuous time activity.

The continuous-time comparators compare continuously the input signal with the reference signal.

The discontinuous-time comparators compare the input signals only at certain time moments, when the output signal is needed by the digital circuit. The time period while the comparator is not used by the digital part of the circuit is named idle period and can be used to improve significantly the comparator's performance.

In the presented article the designed comparator uses the idle period to improve its average power consumption.

Dependent on the means to generate reference voltage, the comparators are classified in two categories: comparators with intrinsic reference voltage and differential comparators.

Many digital circuits need a high speed variation on their input in order to work properly. If the input signal has a slow variation speed a solution to increase output variation speed is to increase comparator's gain. Unfortunately this solution also results in noise and perturbation amplification. Thus, at input signals values near threshold voltage the comparator output will "chatter" (during the transition interval the comparator output switch back and forth many times) and the system doesn't work properly.

The solution to this problem is to introduce the hysteretic comparator with two threshold voltages: one for the **1** to **0** transition and one for the **0** to **1** transition.

The hysteresis voltage of a comparator can be extrinsic or intrinsic and is given by equation (1).

$$V_{hist} = V_{thUp} - V_{thDown} \tag{1}$$

where V_{thUp} is the threshold for the **0** to **1** transition, V_{thDown} is the threshold for the **1** to **0** transition.

If the hysteresis voltage is comparable to the threshold voltages, the comparator is also called Schmitt trigger.

The solution to design a circuit with hysteresis is to use the dominant positive feedback. The positive feedback loop can be added to a comparator without hysteresis or can be placed inside the comparator. The comparators that have an external positive feedback loop are commonly named comparators with extrinsic hysteresis. If the positive feedback is placed inside the comparator the comparator has intrinsic hysteresis.

Figure 1 presents the typical schematic of a non-inverting extrinsic hysteresis comparator. The equations that describe the threshold voltages are given by equations (2), (3) and (4):

$$V_{thDown} = V_{REF}\frac{R_I + R_F}{R_I} - V_{OL}\frac{R_I}{R_F}, \tag{2}$$

$$V_{thUP} = V_{OL}\frac{R_I}{R_I + R_F} + V_{REF}\frac{R_F}{R_I + R_F}, \tag{3}$$

$$V_{Hyst} = V_{thDown} - V_{thUP} = \frac{R_I}{R_I + R_F}\left(V_{OH} - V_{OL}\right), \tag{4}$$

where V_{OH} and V_{OL} are the output voltages for the logic **1** output, respectively, for logic **0** output: V_{REF} is the reference voltage.

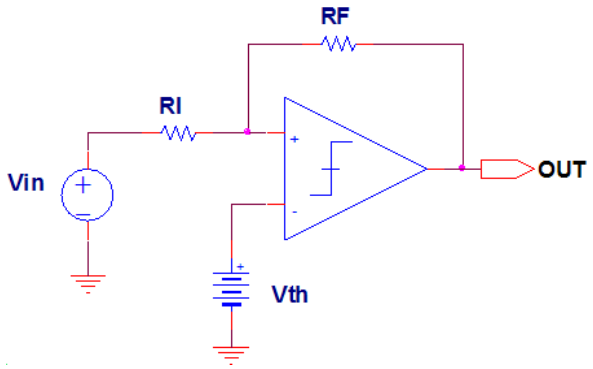

Fig. 1. Non-inverting extrinsic hysteretic comparator.

Figure 2 presents the typical schematic of an inverting extrinsic hysteresis comparator. The equations that describe the threshold voltages are given in equations (5), (6) and (7):

$$V_{thDown} = V_{OH}\frac{R_I}{R_I + R_F} + V_{REF}\frac{R_F}{R_I + R_F}, \tag{5}$$

$$V_{thUP} = V_{OL}\frac{R_I}{R_I + R_F} + V_{REF}\frac{R_F}{R_I + R_F}, \tag{6}$$

$$V_{Hyst} = V_{thDown} - V_{thUP} = \frac{R_I}{R_I + R_F}\left(V_{OH} - V_{OL}\right). \tag{7}$$

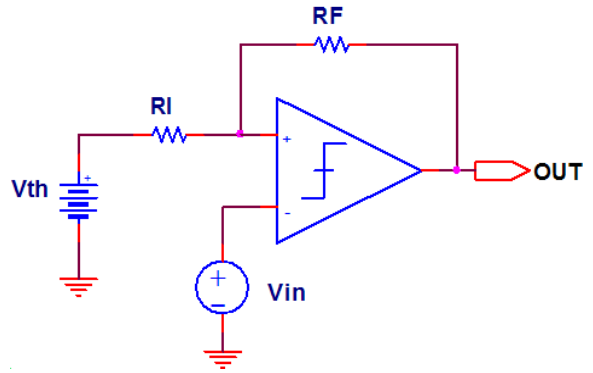

Fig. 2. Inverting extrinsic hysteretic comparator.

2. Methods

The designed circuit is a discontinuous-time, extrinsic hysteresis, non-inverting voltage comparator. Figure 3 illustrates the block schematic of the designed circuit. A D-latch is added in the comparator's loop. The power-on latch logic level is controlled by the *SET* signal. In this case the output of the circuit is set to logic **1** each time the circuit is reset. *SET* signal must be kept low over the entire period while the circuit is working.

The comparator's enable input, *EN*, and D-latch clock input, *C*, share the circuit enable command. When the comparator is enabled the result of the comparison is presented on the D-latch output. A short delay is needed to ensure that the comparator output voltage is stable when the result is stored in the D-latch. The D-latch remains transparent while the enable signal is high and provides at circuit's output the result of the comparison. When the comparator enters shut-down mode, the D-latch clock input is removed immediately and the result remains stored in the latch. This technique will ensure that the comparator will know its previous state when it will enter normal mode again and it will function properly. Using this simple technique the power consumption in shut-down mode becomes zero. The output of the D-latch must have enough strength to drive the current through the feedback resistance and output load. A digital driver should be added on the latch output, to ensure a fast time response.

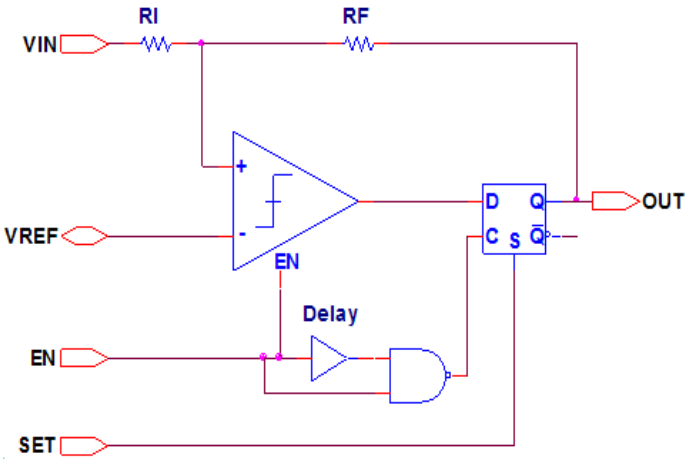

Fig. 3. Status saving comparator block schematic.

The comparator detailed schematic presented in Fig. 4.

The comparator schematic is based on a classical two stage amplifier described in [2] with compensation circuit removed. The comparator was designed in typical 0.18 µm 3.3 V process targeting the following specifications:

- Overdrive voltage: $V_{ovd} = 20$ mV;
- Response time for $V_{ovd} = 50$ mV: $t_r = 0.5$ µs;
- DC current consumption in normal operation mode: $I_Q = 75$ µA;

- Hysteresis voltage: $V_{hyst} = 200$ mV, and
- Reference voltage: $V_{ref} = 1.65$ V.

Comparator's input bias current is 5 µA, and its nominal power supply voltage is 3.3 V.

All transistors, excepting the power off transistors, have the same channel length, $L = 5$ µm while the power off transistor has $L = 0.35$ µm and $W = 1$ µm. The differential pair is biased with a 10 µA current. In order to get a minimal systematic offset the bias current of the second gain stage (transistor MN5) is 20 µA.

In shut-down mode the power-off transistors cut the bias block from the comparator, disable all current mirrors and keep the comparator's output in logic **1**.

Threshold voltages and R_F and R_I resistors values are computed using design requirements and equations (2), (3) and (4):

$$R_F/R_I = 15.5, \quad V_{thDown} = 1.76 \text{ V}, \quad V_{thUP} = 1.55 \text{ V}. \tag{8}$$

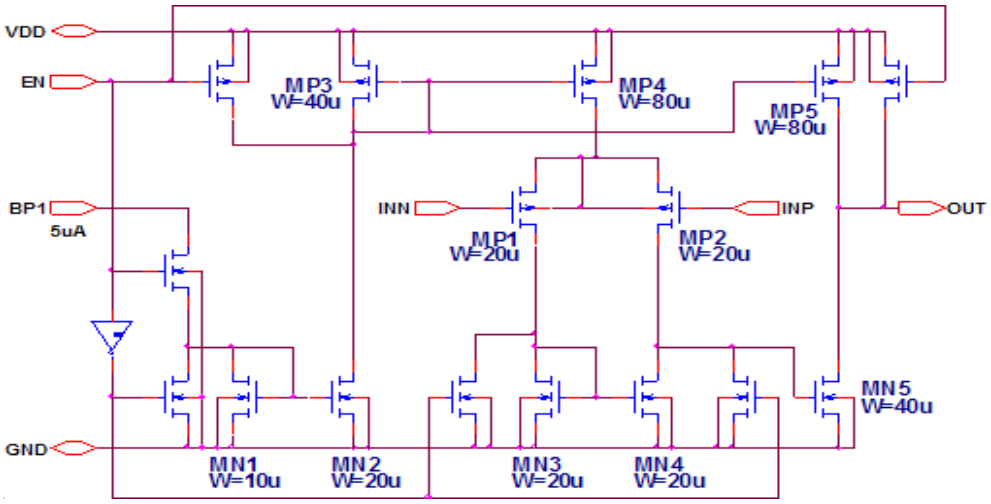

Fig. 4. The detailed comparator schematic.

3. Results

This section presents the H-Spice simulation results of the designed comparator and the impact of the latch on comparator's performances.

The Spice test setup for overdrive voltage measurement is presented in Fig. 5.

The comparator's simulated overdrive voltage is $V_{ovd} \approx 1$ mV. In simulation the random and systematic input offset voltage are neglected. The simulated systematic offset input voltage results as few µV. Random offset will alter the result and overdrive voltage will have higher values.

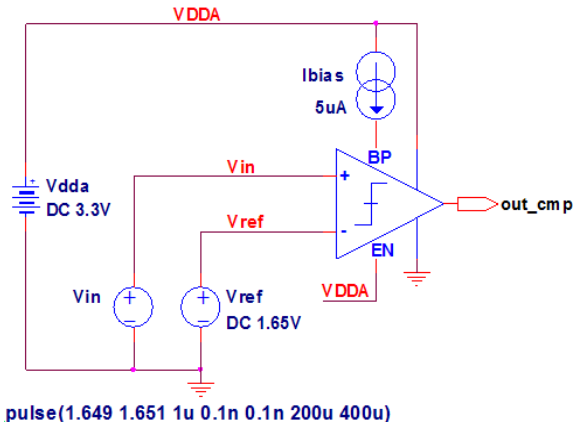

Fig. 5. Overdrive voltage test setup.

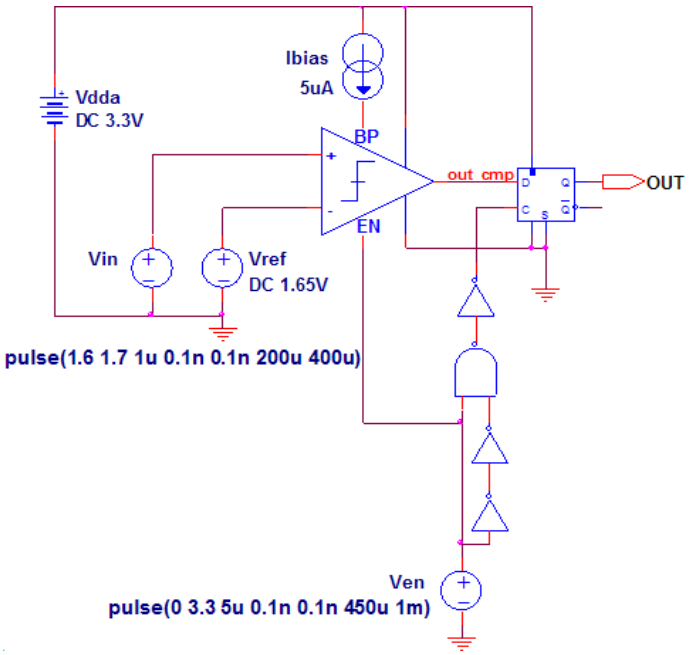

Fig. 6. Response time test setup.

The response time test setup is presented in Fig. 6 and the simulation results in Fig. 7. The comparator's input voltage toggles between 1.6 and 1.7 V ($V_{ovd} = 50$ mV) with a frequency of 2.5 kHz. The enable signal is kept high on the entire period while the response time is evaluated. The simulated response time value is $t_r = 0.18$ µs. As it can be seen, the D-latch doesn't affect the time response of the comparator. The delay between the comparator's output and circuit's output is only 1.5 ns. This delay

value is acceptable for most of today's applications. If a high speed comparator must be used, the delay can be reduced by using a fast response D-latch. The D-latch used in the simulations is obtained from a standard 0.13 um digital library.

Simulation result for DC power supply current of the comparator in normal mode is $I_Q = 56.6$ µA. The digital circuit adds 132 pA, thus the current consumption of the circuit doesn't modify.

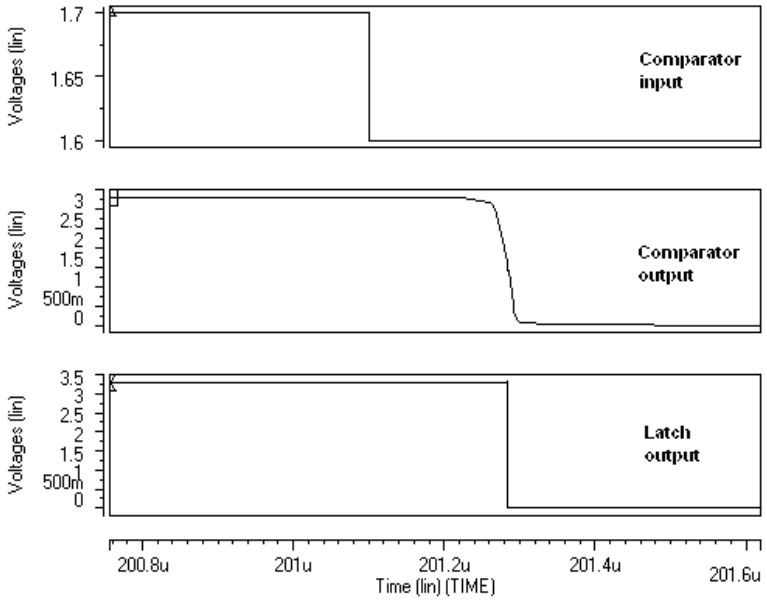

Fig. 7. Response time simulation result.

The complete circuit design and test setup are presented in Fig. 8. Input resistor value is chosen $R_I = 10$ kΩ, and using equation (8) results $R_F = 155$ kΩ. Output and input waveforms of the circuit are presented in Fig. 9.

Normal mode is achieved when *Enable* is logic **1** and shut-down mode when *Enable* is logic **0**. The comparator's input voltage toggles between 0.5 V and 2.5 V ($V_{ovd} = 2.0$ V) with a frequency of 2.5 kHz. The enable signal toggles between 0 V and 3.3 V with a frequency of 1 kHz. The total quiescent current value in normal mode is 56.6 µA. The total quiescent current value in shut-down mode is 206 pA. Namely, the circuit's power consumption in shut-down mode is zero and the comparator's output value is kept unchanged until the next comparison cycle begins.

The equation that describes the power consumption related to the standard comparator is given by (9):

$$\eta[\%] = \frac{I_{QN} D_{EN}}{I_{QS}} \approx D_{EN}, \tag{9}$$

where I_{QN} is the quiescent current of the comparator with state saving, I_{QS} is the quiescent current of the standard comparator and D_{EN} is the duty cycle of the enable signal.

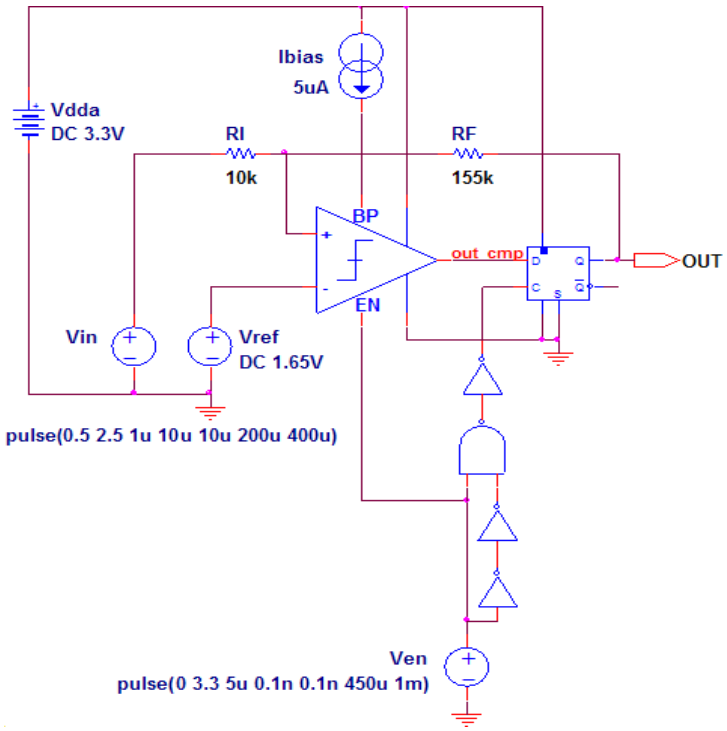

Fig. 8. Hysteretic comparator test setup.

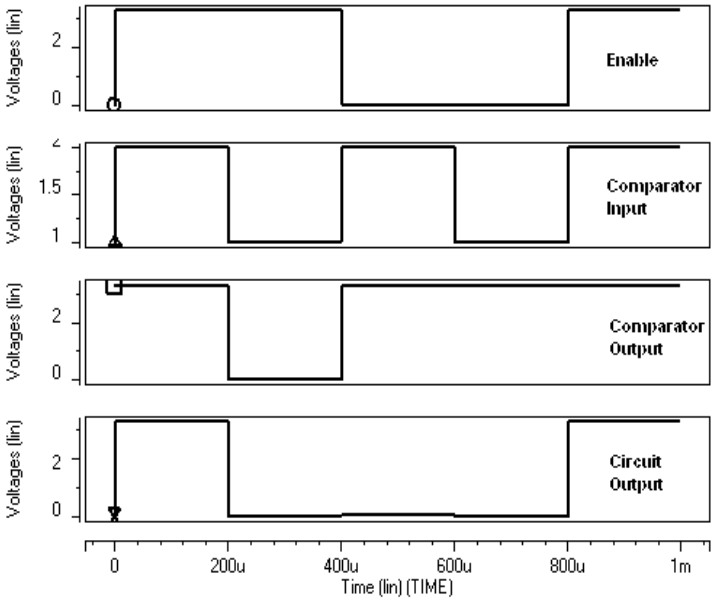

Fig. 9. Hysteretic comparator input and output waveforms.

4. Conclusions

The designed discontinuous-time comparator targeted power consumption reduction. The new design is based on a simple and efficient idea: while the comparator is in shut-down mode, its previous state is stored in a latch.

This design can be used on any existing design to reduce power consumption. Another advantage of the schematic is that it doesn't uses particular devices and can be adapted on any existing CMOS technology.

The circuit has practically no impact if it is used on "already designed" comparators.

A short comparison between the standard comparator and the designed low power comparator is presented in Table 1.

Table 1.

Parameter	**Standard comparator**	**Designed comparator**
Quiescent current Normal mode	56.6 μA	56.6 μA
Quiescent current Shut-down mode	–	206 pA
Response time	180 ns	182 ns

References

[1] Dan C., *Continuous-Time Comparators*, Editura Tehnica, Bucharest, Romania, 2005 (in Romanian language).

[2] Johns D.A., Martin K., *Analog Integrated Circuit Design*, John Wiley & Sons Publishing, 1997.

[3] Maloberti F., *Analog Design for CMOS VLSI Systems*, Kluwer Academic Publishing, 2001.