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Macromodel and Emulator of the Avalanche Gate-Controlled Diode Working in the Analog Regime

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Abstract. This paper presents the simulation results of the gate-controlled diode, working in the analog regime. The aim of the paper is to find the device macromodel that provides an optimum linearity of the junction breakdown voltage versus the gate voltage, at a given current. The lateral pn junction is simulated in the breakdown regime and the gate voltage biases the MOS capacitor in deep depletion. Finally, linearity under 1% was accomplished, being in agreement with the theory. An emulator based on equivalent circuit was developed according to these simulations in order to be implemented in Spice-like programs.

Key words: unconventional MOS device, gated diode breakdown, simulations, equivalent circuit.

1. Introduction

The idea of using the gate-controlled diode working as active component, appeared some years ago, when the influence of a gate control electrode on the breakdown voltage of the pn junction was emphasized, [1, 2, 3]. The typical transfer characteristic is shown in Fig. 1. Increasing the gate voltage, the pn junction breakdown-voltage has a monotone quasilinear variation. This portion of the transfer characteristic is named the analog regime.

At a certain gate voltage (approximately –120V in Fig. 1) another regime appears. This new regime is located in the collapse region where the breakdown voltage suffers

a sharp downfall. Our study is focused on the analog regime, where some applications can be developed, [3, 6].

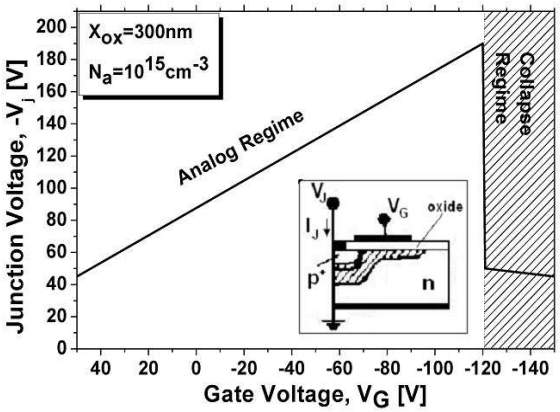

Fig. 1. The transfer characteristics for a gated diode working in breakdown regime at constant reverse current with $N_A = 10^{15}\text{cm}^{-3}$, $x_{ox} = 300$ nm.

2. Simulation results

The device was simulated in the Atlas software. The studied structure has the total size for the silicon region: 15 μm × 15 μm. The discretization mesh was more refined near the Si surface, in order to accurately capture the current flow through the MOS structure.

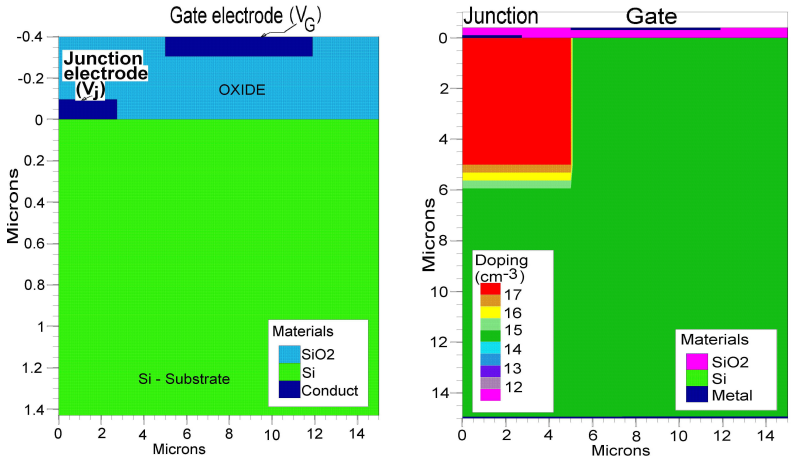

Fig. 2. The device structure: (a) zoom for oxide and electrodes; (b) zoom for the lateral junction.

In a first iteration the gate oxide was x_{ox} = 300 nm thick and the metallization 100 nm. Therefore the minimum y.mesh is located at the coordinate –0.4 μm in Fig. 2a.

Below the oxide, the Si-substrate is defined with a uniform doping concentration about $N_A = 10^{15}\text{cm}^{-3}$. The lateral junction has a constant doping concentration of $N_D = 10^{17}\text{cm}^{-3}$ in the n^+-well and a depth of x_j = 5μm, Fig. 2b. These initial oxide thickness and impurities concentrations were selected in order to compare the simulation results with the performances of an earlier-made experimental structure [4]. The layout was accommodated to actual VLSI dimensions.

The Atlas macromodel for this device includes: SRH model, Boltzmann statistics, SURFMOB model for the carriers mobility, the ionization impact model for the junction breakdown modeling, other breakdown mechanisms (Band to Band tunneling, Fowler-Nordheim, by parameter BBT, NORD).

Figure 3 shows the reverse characteristics of the lateral pn junction at V_G = 2 V, 20 V and 50 V.

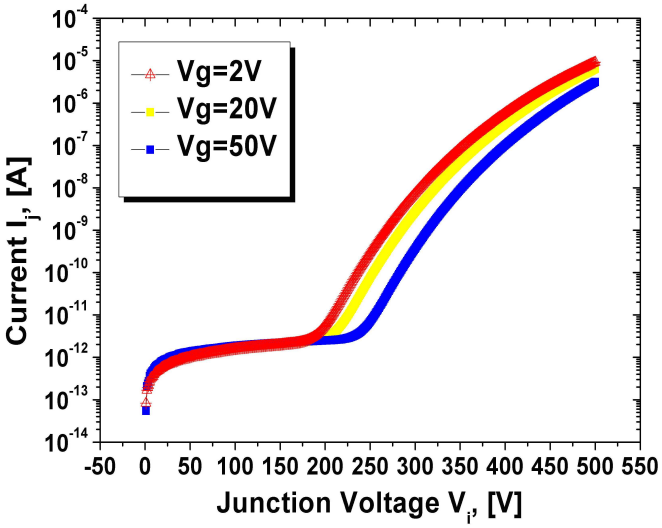

Fig. 3. The reverse characteristics $I_j - V_j$ at distinct gate voltages: V_G = 2, 10...50 V, when$0 < V_j < 500$ V.

The scope is to read the curve $V_j - V_G$ at a given junction current, (*e.g.* $I_j = 2$ μA), as in Fig. 3.

The applied voltage on the lateral junction V_j pushes the device into a breakdown regime with I_j rising, while the positive gate voltage V_G ensures a deep depletion regime for the MOS structure. For a maximum gate voltage of +100 V and a junction voltage of V_j = +500 V, the proof of the simulated potential distribution over the structure is presented in Fig. 4.

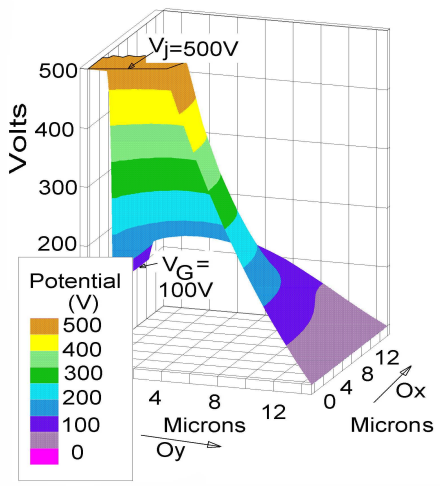

Fig. 4. Potential distribution at $V_G = +100$ V and $V_j = +500$ V.

In Fig. 5, both the junction and gate current were simulated for $0 < V_j < 500$ V. A gate current close to zero proofs that the gate oxide breakdown still doesn't occur.

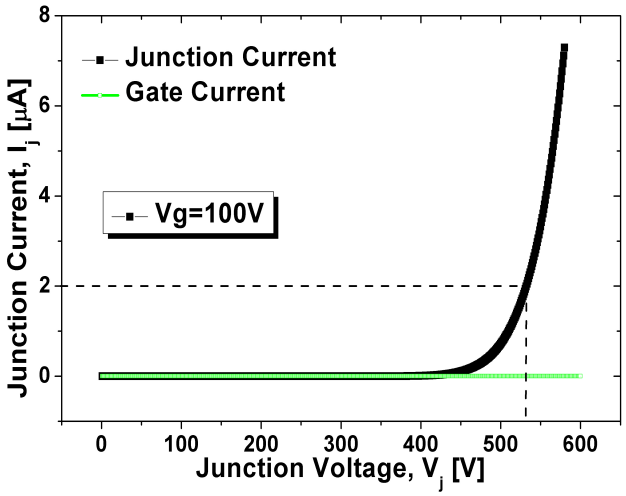

Fig. 5. The junction and gate currents evolution for: 0 V$< V_j <$ 580 V, $V_G = +100$ V with $I_j > 2$ μA.

It is important to limit the gate voltage in order to avoid the oxide breakdown. From this last analysis, the following pairs (V_j, V_G) at $I_j = 2$ μA results as is shown in Table 1. Hence, the increasing monotony of the $V_j - V_G$ function is fulfilled, with linearity under 1%.

Table 1. Some simulated points of the analog regime at $I_j = 2$ μA for a gated diode having $x_{ox} = 300$ nm and $N_A = 10^{15}$ cm^{-3}

V_G	V_j
2	432
20	455
50	485
100	530

3. Optimizations and extensions for simulations

In order to validate the proposed theory, the simulations were extended.

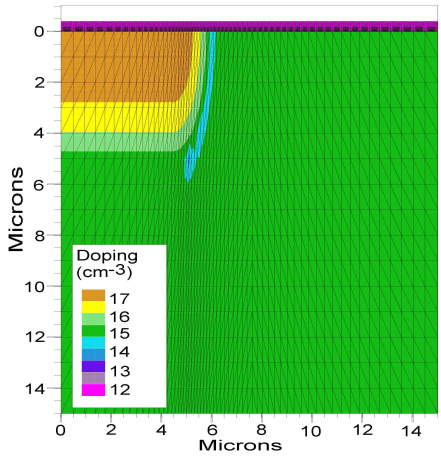

Fig. 6. The final structure adopted for the gated diode.

A first model closer to a real diffused structure admits the Gaussian distribution for the lateral junction doping concentration (Fig. 6).

Within this first gaussian optimization, maintaining $x_{ox} = 300$ nm and $N_A = 10^{15}$ cm^{-3}, the simulations revealed the results shown in Table 2. The corresponding linearity is better than 1.5%.

Table 2. The simulated points of the analog regime corresponding to the same device as in Table 1, having gaussian impurities distribution

V_G	V_j
2	367
20	382
50	410
100	457

Maintaining the gaussian doping concentration profile and the substrate uniform doping at 10^{15}cm^{-3}, the simulations were extended to other values of the oxide thick-

ness: 30 nm and 15 nm. But the gate voltage, V_G, was increased only up to 30 V, in order to avoid the gate breakdown.

Figure 7 proves the situation at $V_G = 2$ V, when the structure has $N_A = 10^{15}$ cm^{-3} and 15 nm oxide thickness. Similar simulations were performed for $x_{ox} = 30$ nm and $N_A = 10^{15}$ cm^{-3}.

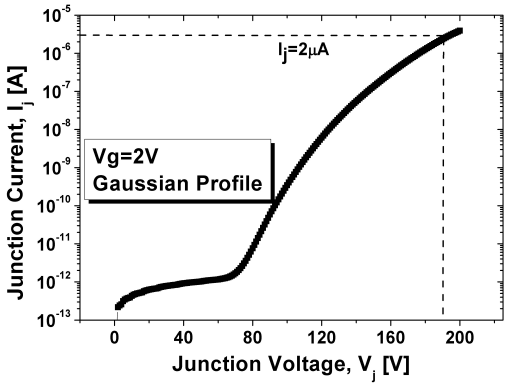

Fig. 7. The junction current simulated for $x_{ox} = 15$ nm and $N_A = 10^{15}$ cm^{-3} at $V_G = 2$ V, when $0 < V_j < 200$ V.

Subsequently preserving the Gaussian doping concentration profile, the simulations were extended to other value of the doping concentration in substrate: $N_A = 10^{16}$ cm^{-3}, maintaining the oxide thickness at 30 nm. The gate voltage was increased from 2 V up to 30 V.

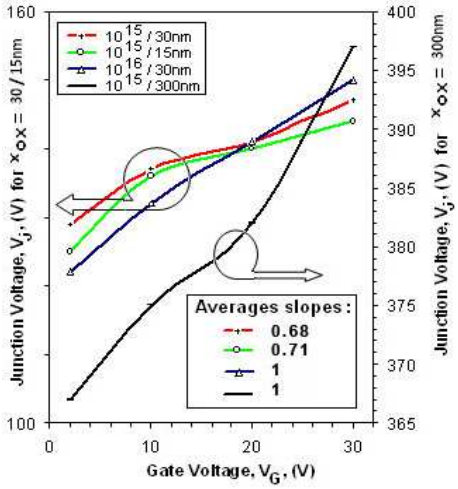

Fig. 8. The transfer characteristics for different substrate doping concentrations and oxide thicknesses.

Figure 8 presents the simulated transfer characteristics for different substrate doping concentrations (10^{15} cm^{-3}, 10^{16} cm^{-3}) accompanied by different oxides thick-

nesses (300 nm, 30 nm or 15 nm). From these plots it can be selected the structures with large portions of transfer characteristics having close unity slope. The inset of this figure presents the calculated average slopes over entire gate voltage game. These values are situated in the interval $1 \ldots 0.68$. The simultaneous reduction of the substrate concentration and oxide thickness maintain the structure far from an ideal one, demanding unity slope of the transfer characteristic.

4. Discussions

The main question arises from the observation that VLSI devices with reduced dimensions lose the principal performance of the analog regime, *i.e.* the unity slope of the transfer characteristic. This result is in strong contradiction with the condition:

$$x_{ox} << W, \tag{1}$$

where W is the width of junction charge space region [1, 5]. The above equation was established for earlier devices with thick oxides and, as consequence, the scaled down ones are recommended for an ideal analog regime. The condition (1) was extracted from the conservation law of the maximum electric field at the oxide-semiconductor interface (see Fig. 9).

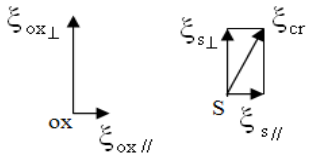

Fig. 9. The maximum electric fields of the p-n junction at the oxide-semiconductor interface.

Inside the semiconductor, the electric field gains the critical value ξ_{cr}. The normal field in the oxide is given by:

$$\xi_{ox\perp} = \frac{V_{BR} - V_G}{x_{ox}}. \tag{2}$$

Considering low values of the lateral fields:

$$\xi_{ox//} = \xi_{s//}, \tag{3}$$

the normal displacement conservation law at the oxide-semiconductor interface gives:

$$K_{ox} \cdot \frac{V_{BR} - V_G}{x_{ox}} = K_{Si} \cdot \xi_{cr}, \tag{4}$$

where K is the dielectric constant. From this equation a unity slope linear variation of the $V_{BR} - V_G$ dependence is obtained.

The strong reduction of the VLSI devices dimensions generates non-negligible lateral electric fields. This is the explanation of the slope far from the unity of the simulated and measured structures [2]. In order to improve this performance, the gate extension over the thin oxides must to be enough large – not reduced to scale – for low lateral electric fields.

5. Emulator of the analog regime

Based on analog regime simulations, an equivalent circuit was conceived in order to be used in Spice-like programs. The paper [4] has presented a such emulator that covers the both regimes, analog and collapse but is restricted to anod-grounded configuration. The present one is dedicated to analog regime only but is designed to work in both configurations, common anode and common cathode . The typical amplifier circuit with load resistances in both anode and cathode electrodes is shown in Fig. 10.

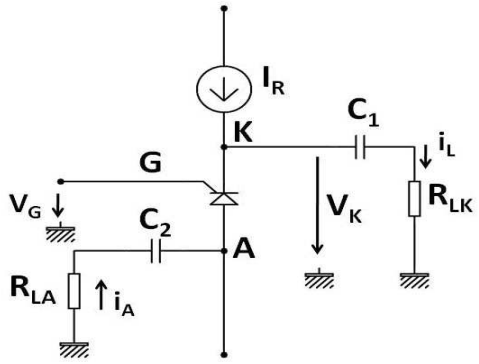

Fig. 10. Typical amplifier circuit with gated diode working in avalanche.

The circuit is biased with a constant current generator, I_R. The unity slope ideal transfer characteristic was demonstrated with the common-anode voltages:

$$V_{KA} = V_{GA} + const. \tag{5}$$

Adding V_A voltages in the both terms of above equation, a similar unity slope characteristic is obtained with the corresponding voltages, V_K and V_A, ground-referred:

$$V_K = V_G + const. \tag{6}$$

A real transfer characteristic is:

$$V_K = mV_G + V_{K0}, \tag{7}$$

where $m \approx 1$ is the slope and V_{K0} – the output cathode voltage for zero-input gate voltage.

The dynamic behavior consists in maintaining the same variations of the cathode and anode currents, as result of very small values of the gate currents:

$$I_A = I_L. \tag{8}$$

The notations for anode load resistance and cathode load resistance are R_{LA} and R_{LK}, respectively.

The emulator of these functions is shown in Fig. 11. It consists in an equivalent circuit made with the operational amplifier TL 084.

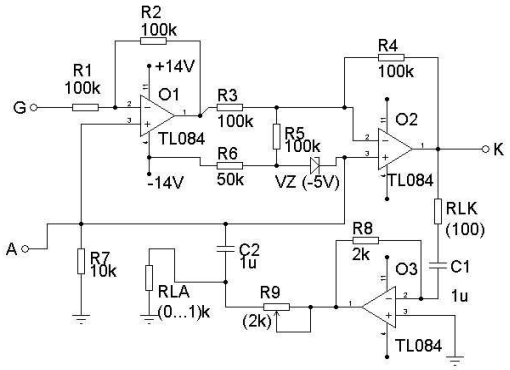

Fig. 11. The equivalent circuit corresponding to analog regime of the gate controlled avalanche junction used in both configurations common anode and common cathode.

The op-amps, O1 and O2, assure the static transfer characteristic:

$$V_K = V_{K0} + mV_G, \tag{9}$$

where:

$$V_{K0} = V_K|_{V_G=0} = V_Z \quad \text{and} \quad m = \frac{R_2}{R_1}. \tag{10}$$

The dynamic function is performed by O_3 op-amp if the condition:

$$R_9 = R_8 - R_{LA} \tag{11}$$

is maintained.

6. Conclusions

Several simulations were made on gated diodes working in avalanche mode, in the analog regime. Many results have denoted quasi-ideal situations when the transfer characteristic have the slope close to unity. It is observed that the use of small thickness oxides (under 30 nm) and/or big substrate concentrations (more than 10^{16} cm^{-3}) diminishes the slope. Unity slope improving can be achieved by keeping enough large the extensions of the gate over the thin oxide. This condition permits the lateral electric field lowering.

An emulator of this regime was designed in order to use the structure in electronic circuits, biased in the common anode or common cathode configurations.

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