

# A Low Switching Time BiCMOS CML Transmitter for High Speed Adaptive Pre-Emphasis Serial Links

Marius GOOSEN<sup>1</sup>, Saurabh SINHA<sup>1</sup>, Alexandru MÜLLER<sup>2</sup>

<sup>1</sup> Department of Electrical, Electronic and Computer Engineering,  
University of Pretoria, South Africa

E-mail: {mgoosen, ssinha}@ieee.org

<sup>2</sup>National Institute for Research and Development  
in Microtechnologies, Romania

E-mail: alexm@imt.ro

**Abstract.** Due to the advances in multimedia applications in recent years, the requirement for high user end bandwidth has increased significantly. The increase in data rates cause jitter requirements to become even more stringent. An adaptive finite impulse response (FIR) filter is proposed to compensate for the non-ideal channel causing data dependant jitter (DDJ), hence improving signal integrity. This paper proposes a current mode logic (CML) based transmitter which incorporates BiCMOS logic, to reduce the rise/fall times of the high speed transmitter. Simulation results of the BiCMOS CML transmitter is presented showing a 30 % improvement in rise/fall times under high current and high output load conditions.

**Key-words:** FIR filter, High speed serial link, CML, BiCMOS, Adaptive pre-emphasis.

## 1. Introduction

The increase in high user end bandwidth applications, such as high definition multimedia streaming, has brought forth a need for higher speed, higher fidelity serial links. High speed serial links provide a high bandwidth solution at a lower cost by reducing the amount of physical pins, hence increasing the bandwidth per pin [1], [2].

High speed serial links suffer from its own set of non-idealities, one of which is jitter. Jitter is defined as the deviation from the expected or ideal timing instant. This timing instant can either be the sampling instant at the centre of the received pulse or at the pulse edges.

Data dependant jitter (DDJ), falling under the category of deterministic jitter, distorts the pulse edges and deteriorates the signal integrity. This paper focuses on printed circuit board (PCB) backplane channels as presented in [3]. The channel bandwidth limitation that is introduced, causing the DDJ, is mainly caused by the chip parasitic components, skin effect (called conductor loss) and dielectric loss. The attenuation of such a channel is simulated to have an attenuation of more than 50 dB at 10 GHz [3]. The frequency dependent characteristic of the channel distorts the different spectral components comprising the transmitted data signal, each with a different amount. Since the spectral components of the transmitted data signal depend directly on the data sequence transmitted, the jitter imposed on the pulse edges is aptly called DDJ.

One way to compensate for the channel bandwidth limitation causing the data dependant jitter is to apply the inverse of the channel response to the transmitted signal. Thus ideally a flat magnitude and linear phase response will be received at the far end of the link.

The inverse of the channel response can be applied to the transmitted signal, boosting the higher frequency components and reducing the long tail in the impulse response, by applying finite impulse response (FIR) filtering. Pre-emphasis has been widely implemented to overcome the data DDJ [1], [2], [4].

Adaptive pre-emphasis allows the transmitter to adapt for any channel without any prior knowledge of the channel response. Externally adjustable FIR filter pre-emphasis as well as adaptive FIR filter pre-emphasis require large chip real estate to implement. This is mainly due to the fact that the driving metal oxide semiconductor (MOS) transistors need to be large to drive the load current at a reasonable rise/fall time.

Complementary MOS (CMOS) did in fact take over from conventional Si bipolar junction transistors (BJTs) for digital circuits in the early 1990's, but the wireless and high data rate wireline domains are another matter entirely [5]. This is due to the far more stringent demands placed on the devices than in simple digital logic. One example of the stringent demands is OC-192 standard requiring less than 10 % jitter per unit interval on the received signal. With a data rate of 10 Gb/s, this results in a jitter requirement of 10 ps.

This paper proposes the design of a high speed serial link transmitter employing adaptive FIR filter pre-emphasis. The transmitter makes use of high speed SiGe heterojunction bipolar transistors (HBTs) as the driving transistors, but it is in turn driven by conventional CMOS logic to achieve a BiCMOS circuit in a CML configuration.

Section 2 introduces FIR filter pre-emphasis in high speed serial links, with a focus on adaptive pre-emphasis as presented in [3] and [6]. Section 3 introduces the design of the high speed serial link transmitter. Section 4 contains the simulation results.

## 2. FIR Pre-Emphasis in High Speed Serial Links

FIR pre-emphasis alters the signal before transmission by emphasizing the high frequency components (pulse edges) of the transmitted signal. Pre-emphasis only requires knowledge of the current and previous transmitted bits, and can therefore easily be implemented with the use of delay elements. These delay elements can either be symbol spaced or fractionally spaced depending on the need. Fractionally spaced FIR filter pre-emphasis requires a larger amount of filter taps, but outperforms the conventional symbol spaced FIR filters [6].

Adaptive pre-emphasis as proposed in Fig. 1, utilizes symbol spaced filter taps. A simple combination of pilot signalling and peak detection is an easy and effective way of applying adaptive pre-emphasis [3], [7].

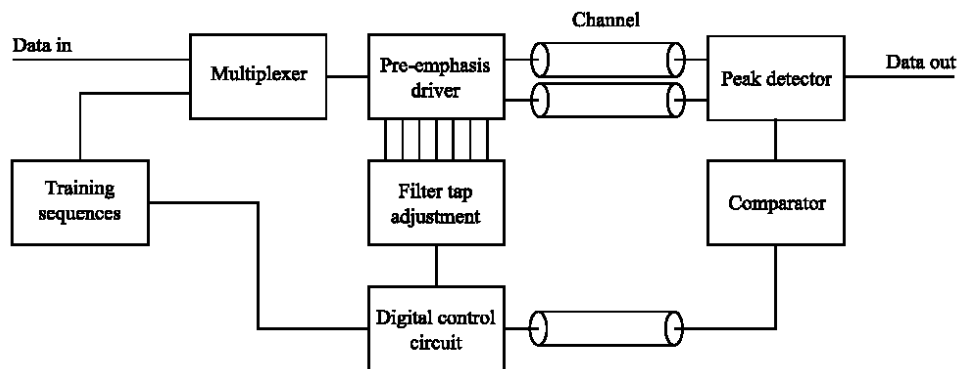


Fig. 1. Adaptive FIR filter pre-emphasis high speed serial link.

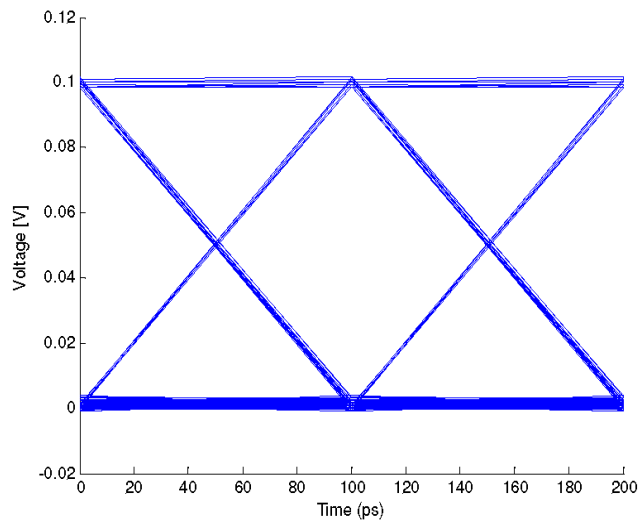


Fig. 2. Data at the far end of the link. Data rate is 10 Gb/s with adaptive pre-emphasis of Fig. 1 applied.

Figure 2 shows the data at the far end of the high speed serial link with adaptive pre-emphasis applied. It should be noted that without pre-emphasis the receiving eye is completely closed.

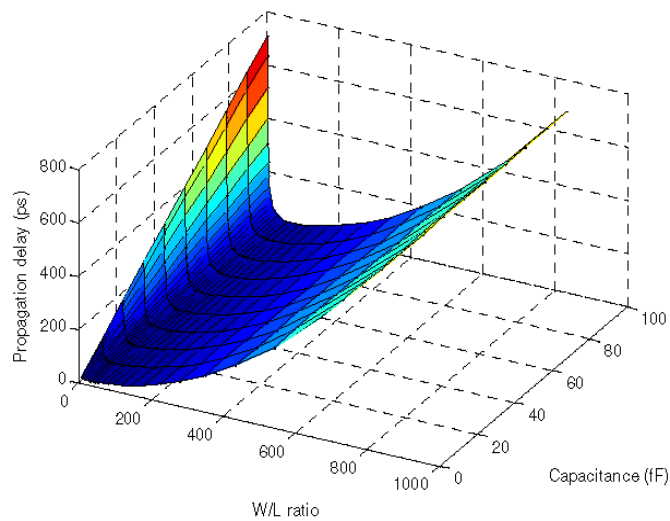
From Fig. 2 it is evident that pre-emphasis is a necessity at high data rates. The adaptive pre-emphasis used is easy implementable but still very effective at high data rates, while requiring only a low frequency return path to alter the tap coefficients to the optimal value. The signal is transmitted as a low voltage differential signal (LVDS) with a typical received voltage level of 100 mV peak. This will require a transmitting signal of larger than 100 mV to compensate for the channel losses.

Practically this is not the case since the output drive transistor needs to drive a complex load (which includes a large capacitance). Section 3 proposes a low rise/fall time transmitter for high speed serial links.

### 3. Transmitter Design

#### 3.1. MOS propagation delay

Typical high speed MOS circuit design entails various trade-offs between speed, transistor size and current drive capability. Scaling of MOS transistors according to Moore's law is a direct result of the effect between reducing the parasitic device capacitance at the cost of a lower device transconductance. Luckily, the parasitic device capacitances scale faster than the transconductance, enabling us to scale down the transistor dimensions even further, hence the trade-off is not too severe.



**Fig. 3.** Tradeoffs between transistor speed and size at various capacitance values.

High speed serial link transmitters drive a complex load, which includes the large I/O pad capacitance. Hence a larger device is needed to obtain acceptable propagation

delay (as well as rise and fall times). Fig. 3 illustrates the trade-off involved (using only a simple inverter driver) between speed and the  $W/L$  ratio (transistor size) at different output capacitance values.

From Fig. 3, using the IBM 8HP process, with a 45 fF load capacitance, results in a minimum propagation delay time of 19.1 ps (19 % of unit interval @ 10GHz) with a  $W/L$  ratio of about 58.

Although the propagation delay is not a problem since only the data stream is sent, (and used to recover the clock for sampling) the propagation delay gives a good indication of the expected rise/fall times.

### 3.2. BiCMOS CML design

High speed serial links rely on the fact that the employed transmitter contributes minimal switching delay to the transmitted data signal. The transmitter rise/fall time does however contribute to the DDJ of the system. Although this contribution to the DDJ is minimal with respect to the contribution of the channel effects, any improvement in this regard is useful.

Current mode logic (CML) is usually employed for its high speed current steering capability. A typical CML transmitter with  $N$  filter taps is shown in Fig. 4.

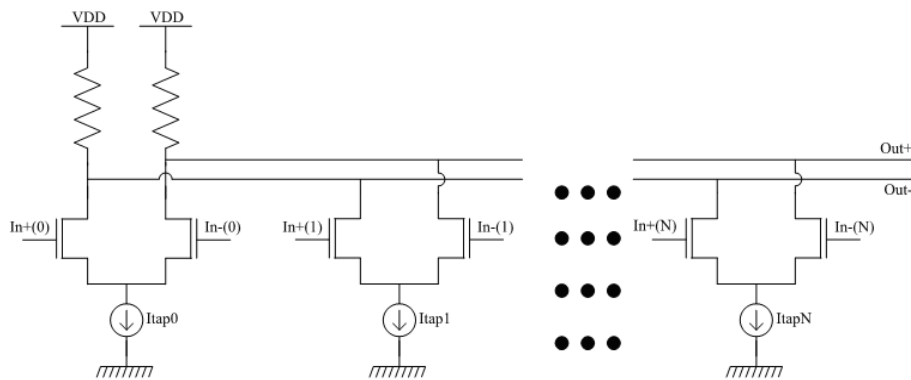


Fig. 4. Conventional CML transmitter with  $N$ -filter taps.

The disadvantage of using a purely MOS CML, also called current controlled CMOS logic or  $C^3$ MOS logic [8], transmitter is the transistor size ( $W/L$  ratio) required to steer the load current. A single filter tap will employ 2 large NMOS transistors to drive the load current, thus for 6 filter taps, as proposed in this study, 12 large NMOS transistors are required.

Thus the number of filter taps that can be implemented becomes directly related to the amount of real estate on the chip.

BiCMOS logic on the other hand makes use of MOS transistors to handle the logic operations (for its negligible static power dissipation) but employ bipolar transistors for the current steering [9].

Bipolar transistors are used for their high current steering capability (large  $\beta$ ), but this comes at the cost of higher static power dissipation (finite base current). The



where  $r_c$ ,  $r_b$  and  $r_e$  are the parasitic collector, base and emitter resistances,  $g_m$  is the half-circuit transistor transconductance,  $R_C$  is the collector resistance,  $C_L$  the load capacitance and  $N$  the amount of filter taps.

The capacitors are defined as in [10]. The expression in (2) is based on conventional transistor models and is suitable for pencil-and-paper design.

#### 4. Simulation Results

Figure 6 shows a comparison between the propagation delay of a single FIR filter tap transmitter as expressed in (2) and the propagation delay as derived from simulation.

As seen in Fig. 6 the expression derived in (2) results in an over-estimation of the propagation delay by about 50 % under ideal driving conditions. The large deviation is due to the fact that the basic transistor model used to derive (2) is not a valid model for high- $f_T$  transistors, but it does provide an analytical expression suitable for a first iteration pencil-and-paper design.

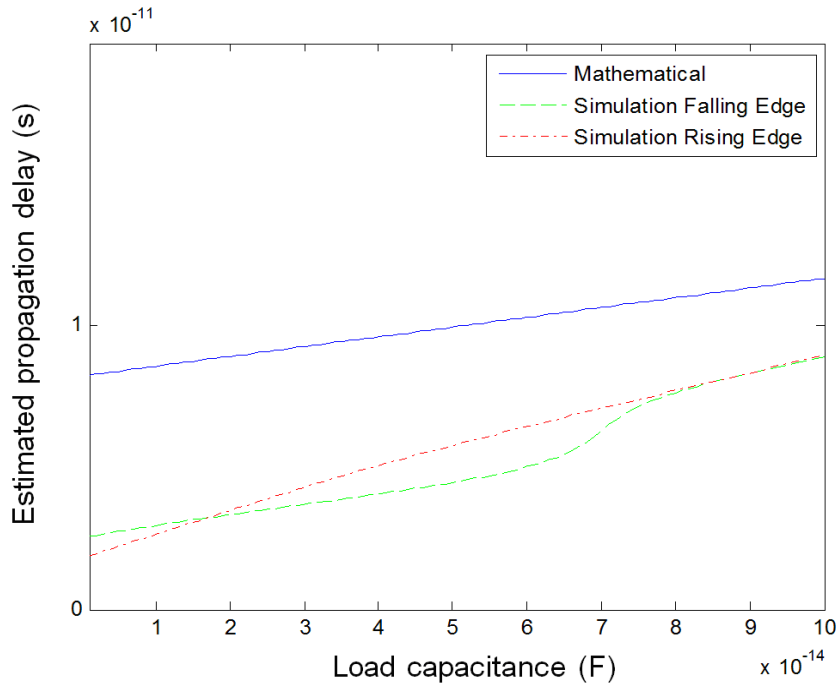


Fig. 6. Comparison between propagation delay derived in (2) and simulation.

Table 1 illustrates the rise/fall time improvement that can be achieved by driving the BCML transmitter with an optimal sized inverter as determined in Fig. 3, hence trading off chip real estate and pulse edge distortion. The optimally sized inverter's aspect ratio is sized to result in the lowest possible propagation with the specific load seen into the base of the HBT.

**Table 1.** Bipolar CML versus C<sup>3</sup> MOS logic rise/fall times

	C <sup>3</sup> MOS	BCML	Optimal C <sup>3</sup> MOS	Optimal BCML
$C_L = 50$ fF $I_{SS} = 2$ mA	32.3 ps	21.2 ps	12.2 ps	13.7 ps
$C_L = 70$ fF $I_{SS} = 2$ mA	32.3 ps	30.9 ps	13.2 ps	14.9 ps
$C_L = 50$ fF $I_{SS} = 5$ mA	32.1 ps	20.3 ps	17.1 ps	11.6 ps
$C_L = 70$ fF $I_{SS} = 5$ mA	50.8 ps	21.2 ps	18.1 ps	12.7 ps

## 5. Discussion and Interpretation

From Table 1 a few key aspects or trends can be noted between the use of BCML and C<sup>3</sup>MOS. The first trend noted is that the rise and fall times of BCML stay relatively constant, whereas the C<sup>3</sup>MOS logic rise and fall times vary slightly more.

This can be attributed to the fact that MOS transistor current depends on both the  $W/L$  ratio and the overdrive voltage ( $V_{ov}$ ). Since the MOS transistor sizing cannot be changed to provide an ideal rise and fall time for every tail current value, the actual rise and fall time as seen in table 1 will be strongly dependent on the change in overdrive voltage. This can be confirmed by looking at equation (3) for the  $g_m$  for a MOS transistor [11].

$$g_m = \mu C_{ox} \frac{W}{L} (V_{ov}), \quad (3)$$

where  $g_m$  is the transistor transconductance,  $W/L$  is the transistor aspect ratio,  $V_{ov}$  is the overdrive voltage,  $\mu$  is the mobility and  $C_{ox}$  is the oxide capacitance. A reduction in current, while keeping the  $W/L$  value the same, requires a reduction in  $V_{ov}$  which results in a linear reduction of  $g_m$ . The unity gain frequency for a MOS transistor can further be expressed as [11]

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd} + C_{gb})}, \quad (4)$$

where  $C_{gs}$ ,  $C_{gd}$  and  $C_{gb}$  are the junction capacitances. Therefore the linear reduction in  $g_m$  results in a direct reduction in  $f_T$ , hence effectively producing a slower MOS transistor.

Thus a few tradeoffs can be considered in designing a fast C<sup>3</sup>MOS logic driver with respect to the optimal transistor size. As shown in equation (3),  $g_m$  depends directly on  $W/L$  while the MOS transistor junction capacitances can be approximated as having a  $W \times L$  term. Hence, to increase the transistor speed the gate length should be reduced accordingly.

Reducing the gate length introduces a few problems affecting the speed of the transistor. These problems can be related to short channel effects.

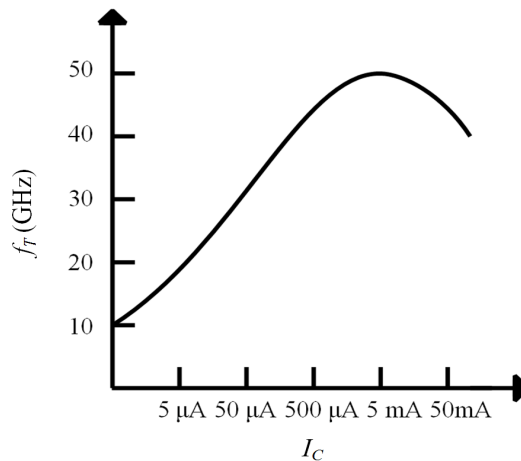
Fortunately the advantages gained from a reduced gate length transistor outweigh the disadvantages, which resulted in the MOS transistor scaling according to Moore's law.

Hence a MOS transistor has a certain  $W/L$  ratio for each tail current resulting in the optimal speed transistor. The transistor can further be fingered resulting in lower output capacitance with regard to a similar sized single finger transistor and hence higher speed, also, only up to a certain finger amount whereby the speed decreases again.

The second trend that can be noticed is that the BCML driver becomes faster at a higher tail current value, while keeping the load the same. This can firstly be seen as having a direct relationship with the unity gain frequency of the HBT. The unity gain frequency for a BJT can be expressed as [11]

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}, \quad (5)$$

where  $C_\pi$  and  $C_\mu$  are the base emitter and base collector capacitances respectively. Since  $g_m$  for a BJT is directly related to the transistor current, an increase in  $f_T$  can be expected. But actually the  $f_T$  of a transistor falls off at higher bias currents because of the decline experienced in the forward transistor current gain. A typical falloff of the unity gain frequency as a function of the bias current is shown in Fig. 7.



**Fig. 7.** Typical unity gain frequency fall off at high bias currents.

This decline in current gain can be attributed to high-level injection and the Kirk effect. Hence it is expected that for a certain process, the  $f_T$  of the transistor will have a peak at a certain bias current as seen in Fig. 7. This is strongly process dependant since it depends on carrier concentrations in the base, collector and emitter. This process dependency can be seen by looking at the data presented in Table 2, which compares a low and high speed SiGe BiCMOS process.

**Table 2.** Bipolar CML rise and fall times for a high  $f_T$  process versus a low  $f_T$  process

	Low $f_T$ process	High $f_T$ process
$C_L = 50$ fF $I_{SS} = 2$ mA	18 ps	13.79 ps
$C_L = 50$ fF $I_{SS} = 5$ mA	24 ps	11.66 ps

The high  $f_T$  process as shown has a peak  $f_T$  value of 180 GHz at a bias current of approximately 5 mA, whereas the low  $f_T$  process peaks at 60 GHz with a biasing current of 600  $\mu$ A. Hence, as can be seen in the data presented in table 2, at a higher bias current with the same load, the actual rise and fall time for the low  $f_T$  process increases with higher bias current. This is in direct contradiction to the high  $f_T$  process which decreases with a higher biasing current due to the peaking behaviour of the  $f_T$  curve.

The high bias current in the low  $f_T$  process can be overcome by adding multiple emitters to the transistor, hence decreasing the amount of current in each and providing a possible  $f_T$  increase for the low  $f_T$  process. However, by adding multiple emitters, the base-emitter capacitance increases which, by looking at equation (2) increases the propagation delay.

## 6. Conclusion

High speed serial links provide a high bandwidth point to point solution for the ever increasing need for high user end bandwidth. Rise/fall times for high speed serial link transmitters determine the ultimate data rate that can be achieved. Using a BCML transmitter, driven by the ideal matching inverter, results in a 30 % improvement in rise/fall time under high current and high load capacitance conditions, which is critical in the primary taps of the transmitter FIR filter. BCML also shows an improvement in the case where the previous stage is not matched to drive the transmitter stage. A high  $f_T$  process was also shown to provide an advantage over MOS transistors for CML transmitters. The high  $f_T$  process also exhibits a higher current operability due to the peaking of the unity gain frequency at a higher bias current.

**Acknowledgments.** The authors would like to thank ARMSCOR, the Armaments Corporation of South Africa Ltd, (Act 51 of 2003) for sponsoring this study.

## References

- [1] BICHAN M., CARUSONE A. C., *A 6.5 Gb/s backplane transmitter with 6-tap FIR Equaliser and variable tap spacing*, Proc. of IEEE custom ICs conf., pp. 611–614, San Jose, 13–16 Sept. 2008.
- [2] TONIETTO D., HOGEBOON J., BENSOUANE E., SADEGHI S., KHOR H., KROTNEV P., *A 7.5 Gb/s transmitter with self-adaptive FIR*, Proc. of IEEE symp. on VLSI circuits digest of technical papers, Honolulu, pp. 198–199, 18–22 Jun. 2008.

- [3] GOOSEN M. E., SINHA S., *Adaptive FIR filter pre-emphasis for high speed serial links*, Proc. of South African conf. semi- and superconductors (SACSST), Cape Town, pp. 37–42, 8–9 April 2008.
- [4] LI M., KWASNIEWSKI T., WANG S., TAO Y., *A 10 Gb/s transmitter with multi-tap FIR pre-emphasis in 0.18  $\mu\text{m}$  CMOS technology*, Proc. of the 2005 IEEE Asia south pacific design automation conf., Shanghai, pp. 679–682, 18–21 Jan. 2005.
- [5] CRESSLER J. D., NUI G., *Silicon germanium heterojunction bipolar transistors*, Artech House, Massachusetts, 2003.
- [6] LI M., KWASNIEWSKI T., WANG S., TAO Y., *FIR filter optimisation as pre-emphasis of high speed backplane data transmission*, Proc. of IEEE Int. conf. on communications, circuits and systems, Chengdu, Vol. 2, pp. 773–776, 27–29 Jun. 2004.
- [7] YOO K., HAN G., *An adaptation method for FIR pre-emphasis filter on backplane channel*, Proc. of IEEE Int. Symp. on Circuits and Systems, Island of Kos, pp. 5151–5154, 21–24 May 2006.
- [8] HAIRAPETIAN A., *Current controlled CMOS logic family*, United States Patent 7215169B2, 8 May 2007.
- [9] KANG S., LEBLEBICI Y., *BiCMOS logic circuits*, in *CMOS digital integrated circuits: Analysis and design*, 3rd edition, McGraw Hill, New York, 2003.
- [10] ALIOTO M., PALUMBO G., *Highly accurate and simple models for CML and ECL gates*, IEEE Trans. on computer-aided design of ICs and systems, Vol. 18, No. 9, pp. 1369–1374, Sept. 1999.
- [11] GRAY P. R., HURST P. J., LEWIS S. H., MEYER R. G., *Analysis and design of analog integrated circuits*, Fourth edition, John Wiley and Sons Inc., New York, 2001.