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A Matching Network Free Approach in Designing Inductorless Low Noise Amplifiers with Programmable Gain for FM-Radio Receivers

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Abstract. In this paper an approach in designing Low Noise Amplifiers suitable for usage in FM-Radio receivers without a matching network is presented. The LNA presented in this paper is implemented in a standard 60 nm RF process. The matching network-free approach is meant to minimize the overall PCB cost of the FM Radio Receiver. In order to eliminate the matching network the input impedance of the LNA is designed to be in accordance with the antenna impedance. The presented LNA has a total gain of 27 dB, programmable in 1 dB-step, in the FM-Radio bandwidth. The noise figure of the LNA is 2 dB, its P1dB is –27 dBm and the current consumption is 3mA.

1. Introduction

FM Radio receivers and even transceivers are beginning to be integrated on a large scale in more and more portable devices. These days FM Radio reception is beginning to be viewed as a standard feature for every portable wireless device on the market. This means that the FM Radio receiver is viewed as a mass produced component. Mass production means the necessity of a cheap and reproducible process. Recently Programmable Gain Low Noise Amplifiers (PGLNAs) in CMOS processes have been studied; nevertheless a small effort in supplying some topologies for the FM Radio bandwidth has been recorded.

This paper focuses on an approach in designing FM Radio LNAs without matching networks. This approach is suitable whenever cost reasons are involved. Due to the

fact that a matching network means the addition of usually two extra components on the PCB where the receiver is mounted, the manufacturing costs of the device will increase. When focusing on creating low cost devices, the production cost of said devices becomes a significant issue.

This approach is exemplified with an LNA circuit which is supplied at 1.5 V. The LNA is designed in a standard 60 nm RF CMOS technology and is suitable for FM radio receivers. The exemplified LNA has digitally programmable gain, switchable in 1dB-steps. For conserving area on the chip, the LNA is designed with a resistive load, which means that the inductor, an omnipresent component in RF circuitry is not used. Today, inductorless LNAs are starting to gain ground in RF designs, but too few studies have been recorded [3].

2. Circuit design

The LNA circuitry is comprised out of two gain stages. In Fig. 1 is shown a concept diagram of the LNA [2]. This cascaded topology assures a satisfactory gain range together with a low input referred noise. Also, separating the circuit into two stages makes the design easier regarding the common mode levels. The first and second stage can have their own, conveniently chosen, input common mode level. Another advantage is that using this topology, the output common mode level can be easily set. This is critical because usually, in a receiver chain, the LNA is fed directly into a mixer. If these two circuits are DC coupled, than the LNA will impose the input common-mode of the mixer.

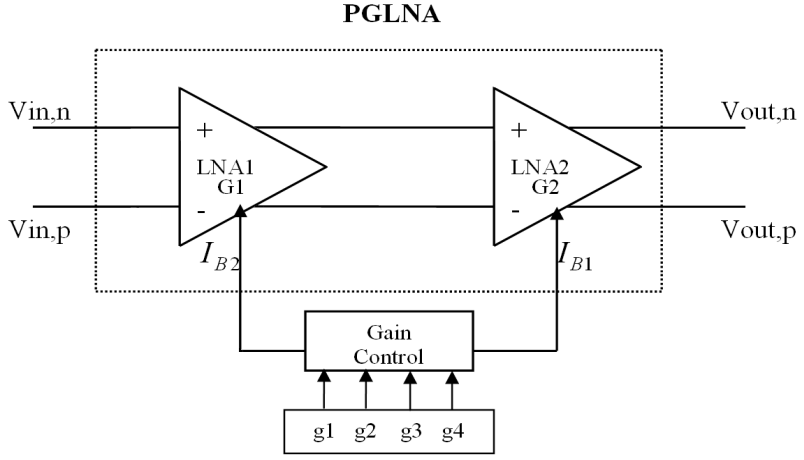

Fig. 1. Simplified schematic of the designed LNA.

Usually mixer topologies are very sensitive with respect to their input common mode, so a precise control of the common mode is required.

A detailed schematic of an LNA gain stage is presented in Fig. 2. As it is explained in detail in [2], the stage includes an output sub-amplifier, an input sub-amplifier and an adjustable bias stage. The operational amplifier used in a negative feed-back loop

sets the common-mode output voltages at the V_{out_p} and V_{out_n} nodes to V_{ref}. Usually for ease of designing the entire receiver chain, we set $V_{ref} = V_{dd}/2$.

The purpose for the PGLNA's gain is to achieve a range of 16 dB in 1 dB steps over the whole FM Radio bandwidth. In figure 2, the Gain Control Block imposes the gain of that stage via 4 control bits in a thermometric code, by adjusting the bias currents of that block. The gain of the amplifier is $G = g_{m1} \cdot R_B$, where $R_B = R_{Bn} = R_{Bp}$.

In general, an LNA with a reasonable Noise Figure (which is around 2 dB) has a current consumption between 5 and 8 mA. From the simulations conducted on this topology, a noise figure of 2.7 dB has been observed for a current consumption of 3.1 mA.

In an RF receiver the input signal is usually provided by an antenna. In the case of FM Radio receivers included in mobile phones and devices, the antenna is actually consisting of the cables of the headphones which are connected to the devices and through which the listening is achieved. This means that the FMR receiver doesn't have its own dedicated antenna. This is an important fact in designing FMR LNAs.

The disadvantage here is given by the impedance of this antenna which varies a lot depending on the shape and position of these wires. From measurement results we have observed that this impedance varies between 50 Ω – 200 Ω for a stretched wire. In the case of a curled up wire, its impedance varies between 30 Ω – 300 Ω. The antenna impedance and its variation are very large. LNAs are fairly sensitive to the impedance present at their input which means that the antenna impedance is an important criterion in designing this LNA.

The problem which arises here is that in the case of a very small useful input signal, such a large variation of the input impedance leads to a large variation of the amplitude of the input signal (which is with respect to the input impedance). In order to have a good rejection of the blockers situated in the GSM bandwidth it is necessary to obtain a good P1dB, around the value of –30 dBm (1 μW). Usually amplifiers have fixed input impedance (which evidently varies with the gain step setting), a fact which can prove to be very harmful because a –30 dBm input signal over a small input impedance in conjunction with a very large gain setting leads to the rapid saturation of the amplifier.

As mentioned earlier, it would be ideal to construct the LNA by using two cascaded gain stages like the one in Fig. 2. This has some disadvantages. The first disadvantage for using the topology in Fig. 2 as an input stage is that its input is differential. In the case of a FMR receiver, the signal provided by the antenna is unbalanced. This means that if we use this stage as an input stage we double the current consumption for achieving a thing which can be reached by using an unbalanced stage with maybe even better performance. If we use a differential input stage for an unbalanced signal it is mandatory to short one of its inputs to the ground. This means that besides the doubled current consumption, we have to use up a lot of chip area for a significantly sized decoupling capacitor.

The requirements also include that the input of the amplifier is coupled to the antenna via a 1 nF capacitor. To reduce cost, a matching network isn't taken into consideration. This means that the input stage must be carefully chosen so that its input impedance is matched from the beginning as good as possible to the an-

tenna impedance. This is kind of tricky because a CMOS input stage has the input impedance of a CMOS transistor which is actually quite a big impedance with a significant capacitive component.

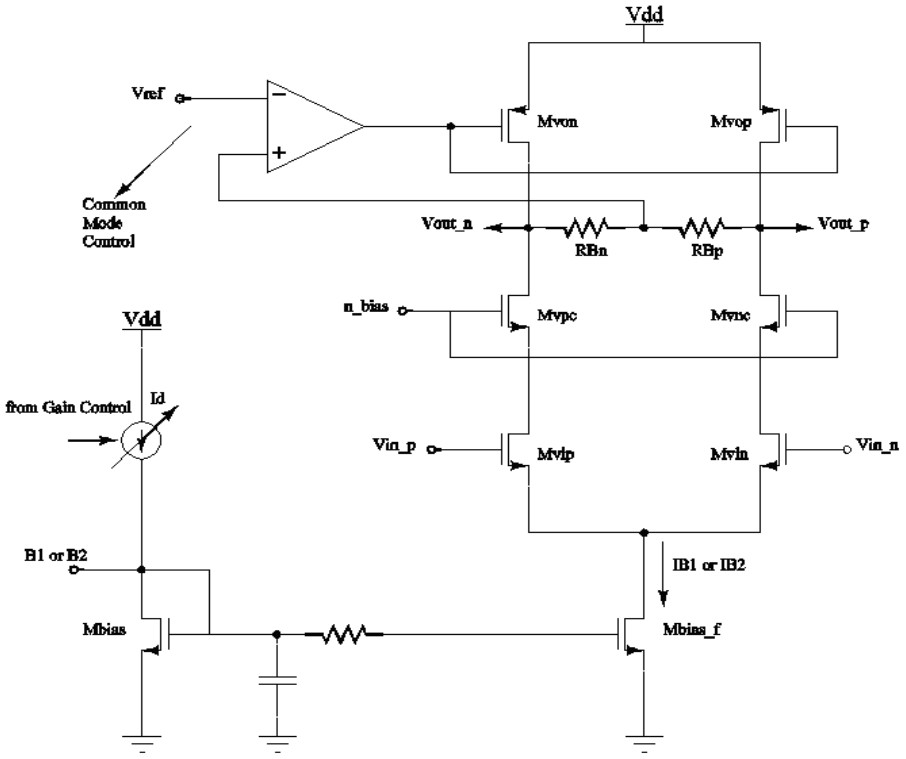

Fig. 2. Transistor level schematic of an LNA gain stage.

In conclusion, if we sum up the requirements for the input stage we can elaborate that: it must be an unbalanced stage, the current consumption and the noise introduced must be minimum, it has to have the input impedance around 200 Ω and a gain as large as possible.

The gain of this stage must be as large as possible and its noise must be as small as possible because in an LNA the noise introduced by the input stage dominates the overall Noise Figure. In general, when referring to the second stage (the output stage in this case), its noise contribution is smaller compared to the input stage because at its input the signal already has large amplitude.

The most convenient topology for use as an input stage is the cascode configuration (Fig. 3), which combines the advantages of two basic amplifiers.

In Fig. 3a, the first gain stage is made up of transistor N2 in common source connection which provides a large gain. The second stage is made up with transistor N3 in common gate configuration which behaves very well with frequency and it provides low noise. The two advantages combined lead to a circuit with a large gain,

a very good circuit behavior and a low noise. The most important thing at this stage of the design is the input impedance.

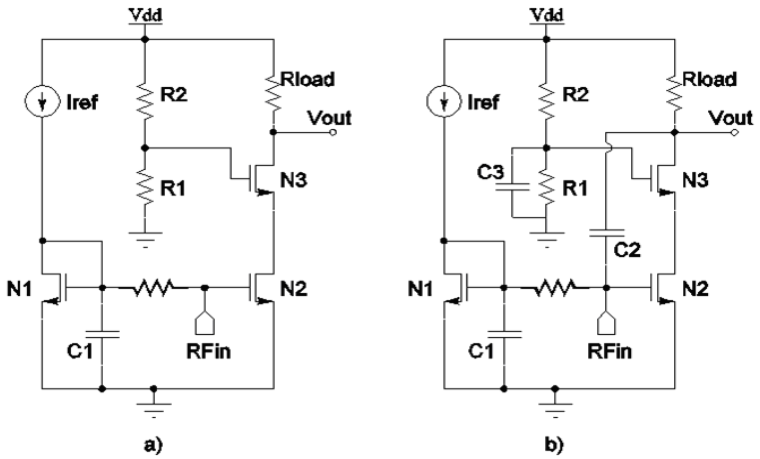

Fig. 3. LNA Input stage schematic.

In Fig. 4, the cascode's input impedance versus frequency is plotted. As it can be observed, the input impedance is not in the range needed. To be well matched at the input we need an input impedance of 200 Ω. The impedance in Fig. 4 is with an order of magnitude larger than what we need it to be.

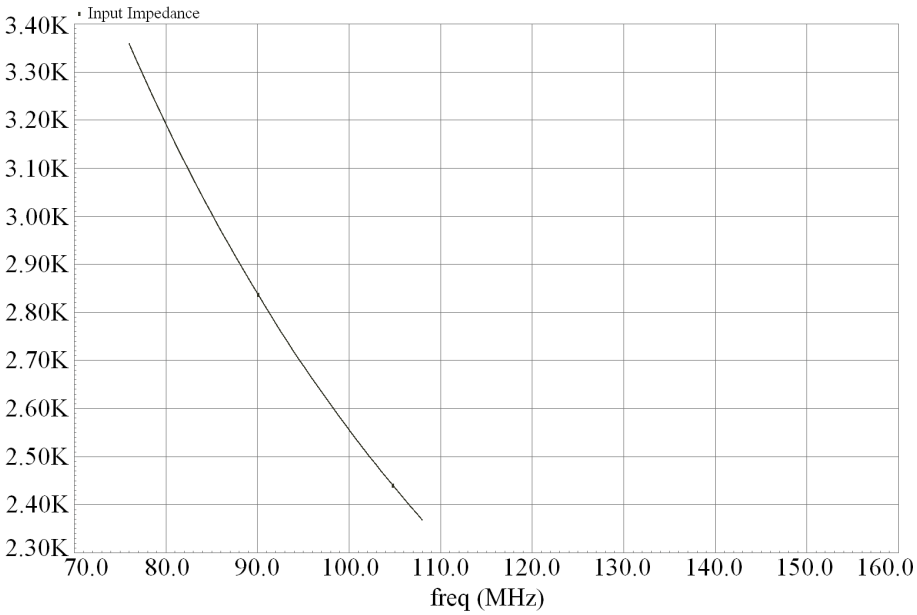

Fig. 4. Cascode Input Impedance.

That's why, in Fig. 3b, a Miller capacitor C_2 has been introduced between the input and the output of the stage. This decreases a lot the input impedance and by properly dimensioning of the devices we can adjust it around the value of 200 Ω to match it with the impedance of the antenna.

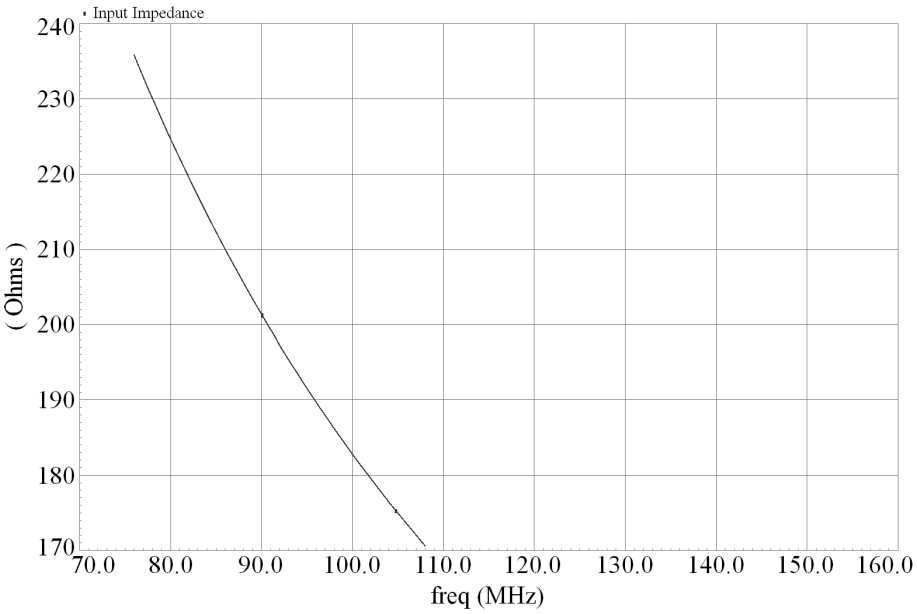

Fig. 5. Input Impedance of the cascode with the Miller capacitor.

3. Simulation results

In this chapter the simulation results of the LNA circuitry are presented. The simulator used was *SpectreRF*. With the previously described building blocks, we can construct the complete PGLNA as it is shown in figure 6. The input stage of the LNA (the cascode in Fig. 3b) is connected to an output stage (shown in Fig. 2). This output stage has an input shorted to the ground via the decoupling capacitor $C4$. This stage is used as an output stage because we need the LNA output to be differential. For biasing the input of the differential output stage, a resistor *(RBias_diff)* has been used. Its value is rather large, it's order of magnitude being in the range of tens of Kilo Ohms, in order not to influence the performance of the stage. The previously mentioned decoupling capacitor, $C4$, has to role of short circuiting, in AC, the input *Mvin* of the differential output stage. By doing this, we obtain a pseudo-differential output signal in the complete LNA. The reason for this is that, because of cost reasons, a un-bal block is not used on the PCB at the input of the LNA.

The disadvantage of this approach is that the amplitudes of the signals seen at the *Vout_n* and *Vout_p* outputs are not equal. This is due to the fact that the *Mvip* transistor functions in common-source connection in the differential stage, and the

Mvin transistor functions in common-gate connection in the same stage. Because the gains of two identical transistors in different amplifier connections are different, this leads to an asymmetry of the balanced output signal. Nevertheless, in FM Radio receivers, this asymmetry doesn't represent a significant issue.

The gain of the complete LNA is varied by varying the bias current of the output stage. This means that for any gain step, the input stage's performance remains unchanged. The advantage in this case is that for any gain setting, the input impedance will remain unchanged, centered on the 200 Ω value, thus always being matched to the antenna.

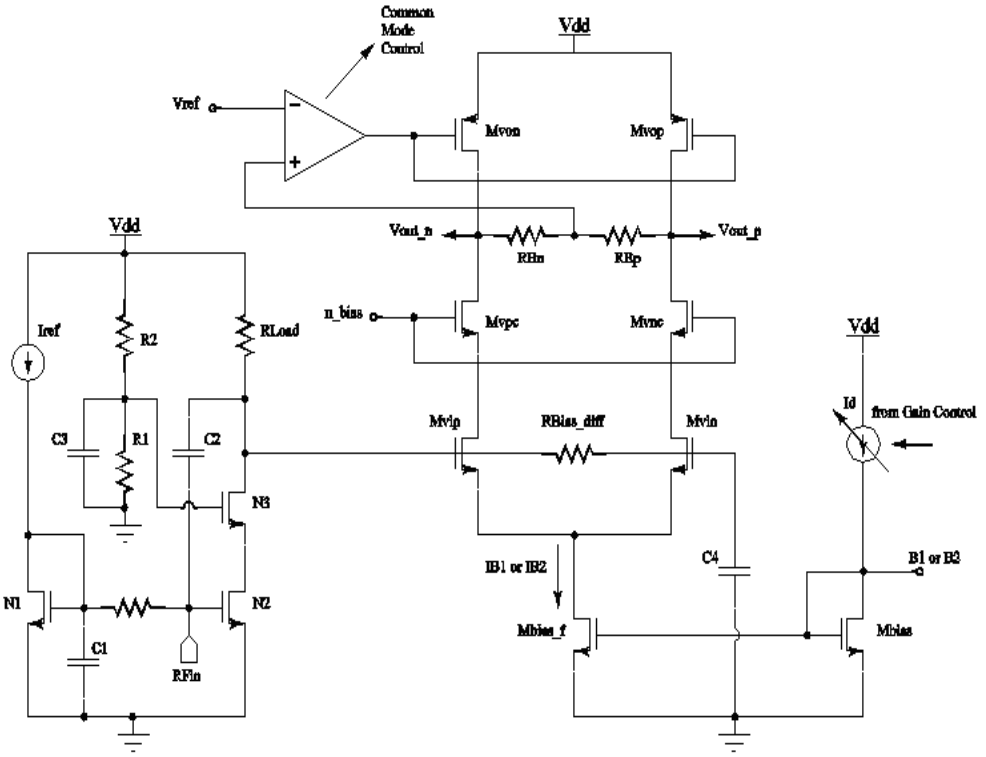

Fig. 6. The complete schematic of the LNA.

In Fig. 7 the gain of the complete LNA is plotted versus frequency. In the bandwidth of interest, which is between 87 and 108 MHz, we can see that the gain has a value of 27 dB. As we can observe from this figure, the gain characteristic is constant in the bandwidth of interest.

In Fig. 8 the LNA Gain steps are plotted. The gain setting is varied digitally with a thermometric code. As it can be observed, there are 16 steps, each one of a magnitude of 1 dB. The gain is designed to vary in the bandwidth of interest from 11 dB to 27 dB. The digital algorithm implemented in the microcontroller decides the gain setting in accordance with the power of the input signal.

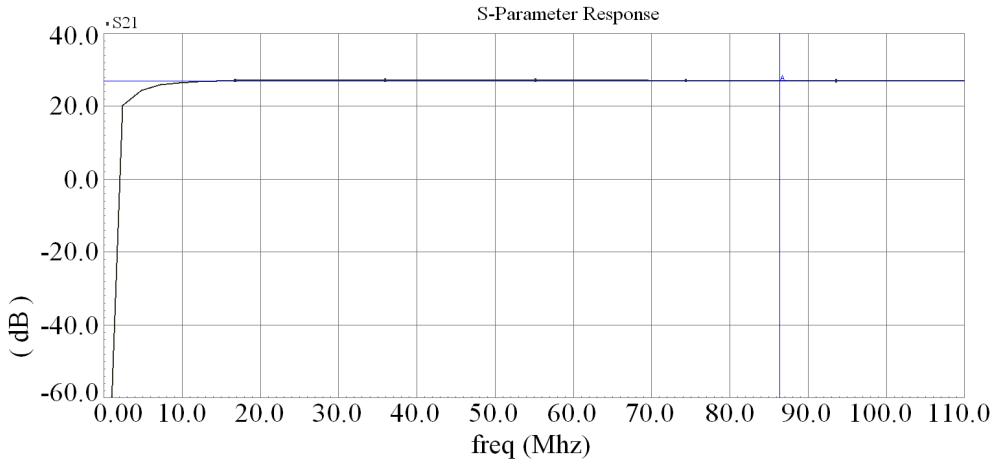

Fig. 7. Total Gain of the LNA.

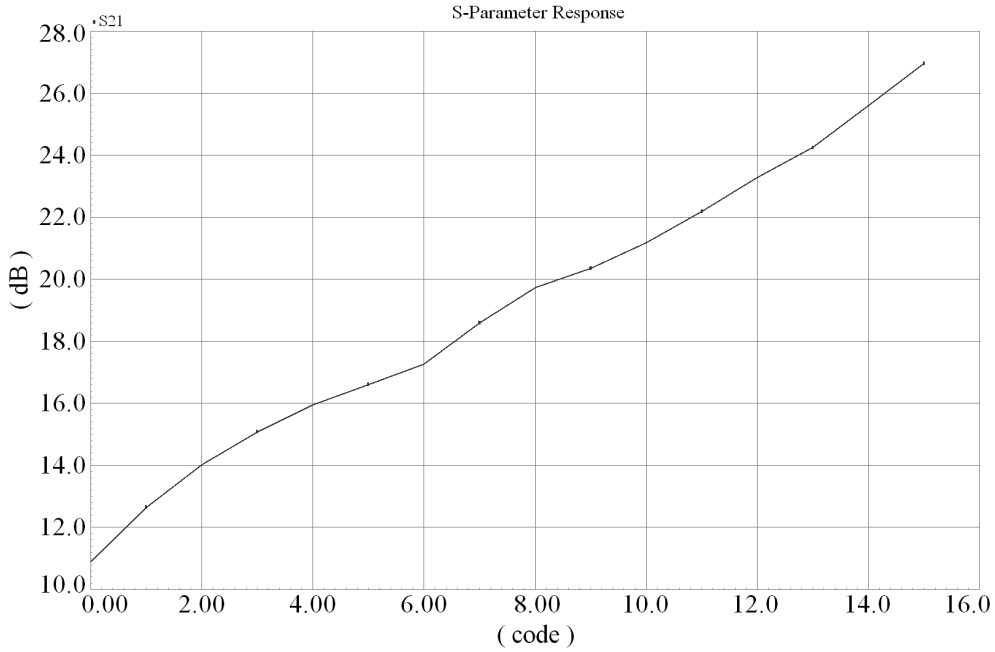

Fig. 8. LNA Gain Steps.

In Fig. 9 the LNA noise figure is plotted. This is a critical parameter for an LNA. From here we can see that in the bandwidth, the maximum noise figure of this LNA is 2 dB.

In Fig. 10, the P1dB of the LNA is plotted. For FMR applications, the LNA should have a minimum P1dB of –30 dBm. From there, we can observe that the P1dB of our LNA is situated at the value of –26.64 dBm.

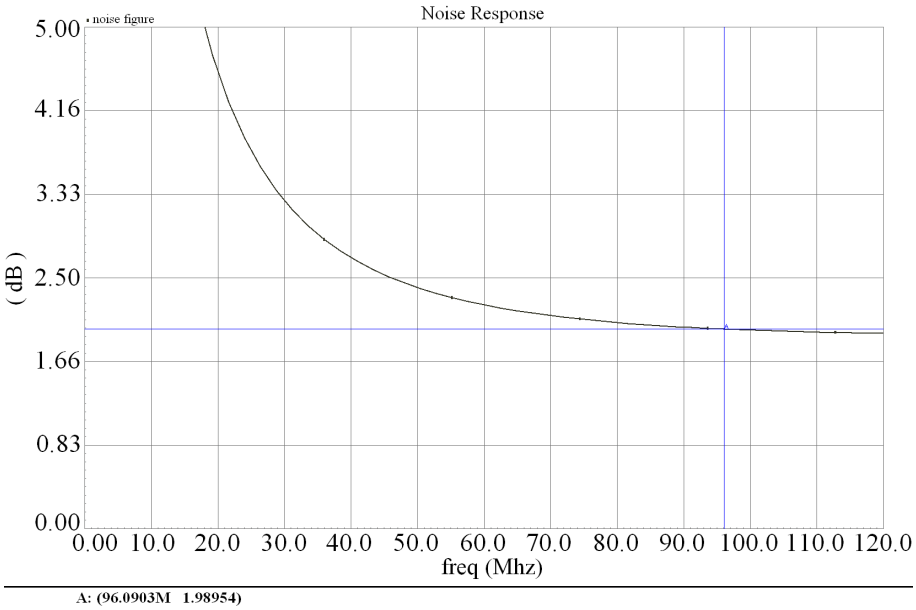

Fig. 9. Noise Figure of the LNA.

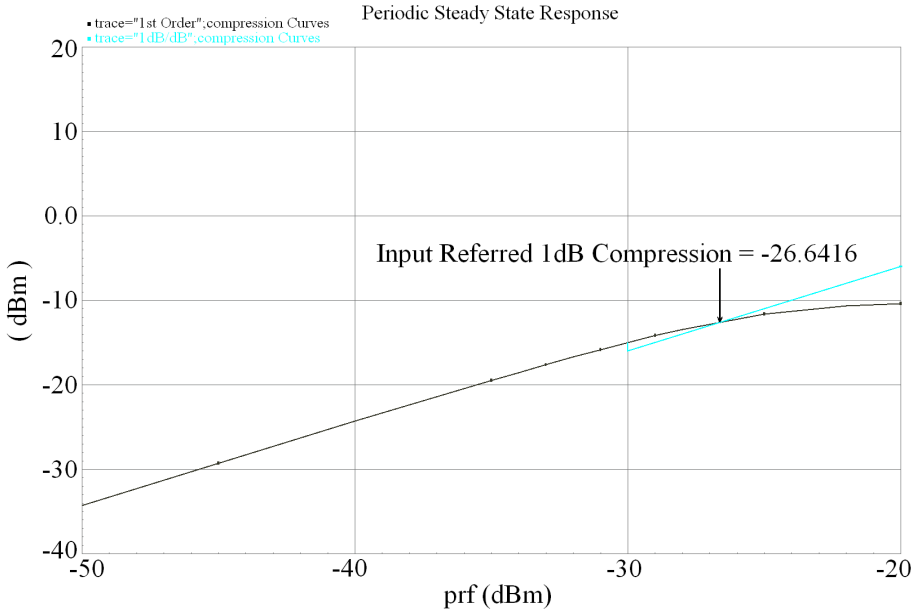

Fig. 10. P1dB of the LNA.

In Fig. 11, the input IP3 plots are shown. As we can see from the simulation results, for this LNA, the IIP3 has a value of –19 dBm, a value which is acceptable.

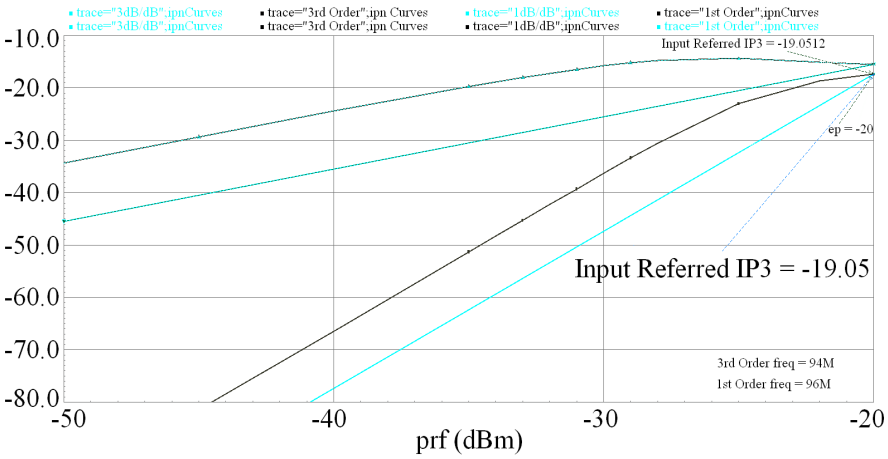

Fig. 11. IIP3 of the LNA.

3. Measurement results

Due to the fact that the FM receiver chip has but one test pin, measurements can be performed on a limited number of parameters. In Fig. 12, the input P1dB and IIP3 measurement results are plotted. As we can see, the measured P1dB has a value of –30 dBm and the IIP3 has a value of –19.5 dBm. Knowing from theory that the value of the IIP3 is usually larger with approximately 10dB than the value of the P1dB, judging by this numbers, we can say that the measurement setup is correct.

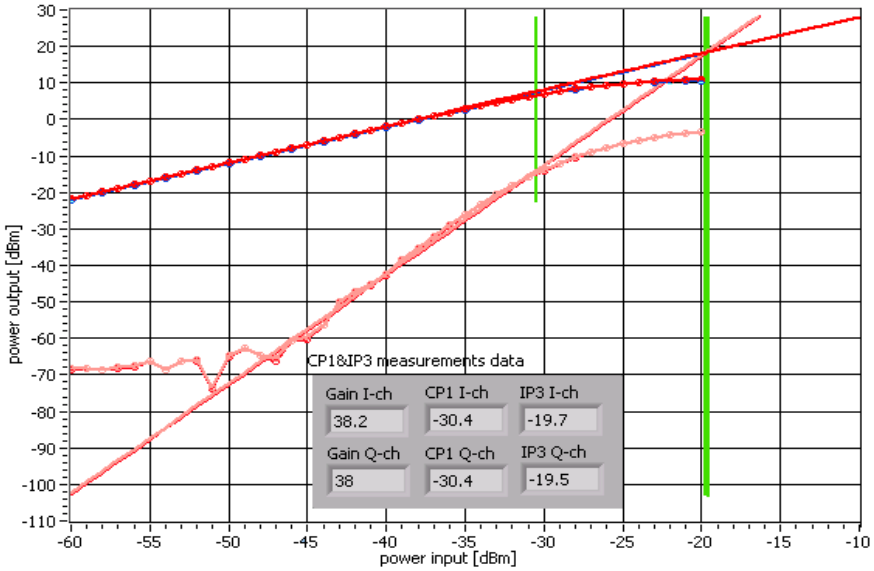

Fig. 12. The measured P1dB and IIP3 of the LNA.

4. Conclusions

In this paper we implemented an innovative resistive load LNA, suitable for FM Radio receivers. At a 1.5 V power supply, the circuit shows a gain of 27 dB, programmable in 1dB-step and a Noise Figure of 2 dB. The input stage of the LNA is designed in such a way that the circuit doesn't require input matching for the antenna. This is done by designing the input impedance to be around the value of 200 Ohms. The circuit exhibits a very good P1db, situated at the value of –26.64 dBm and an IIP3 of –19 dBm. A differential output along with a 3 mA current consumption makes this LNA a good choice for a FM Radio receiver.

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