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Arguments for The NOI Nanotransistor Affiliation to The FETs Family

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Abstract. Among the nanodevices, the vacuum nanotransistors are intensively studied in the last decade. A recent novel device was proposed as the NOI - Nothing On Insulator - nanotransistor, inspired from ultrathin SOI devices. Therefore, this new device preserves some properties from the SOI structures. Obviously, the NOI nanotransistor is a vacuum tunnel device among the vacuum field emission devices. But the main target, in this paper, is to prove that its particularity comes from affiliation to the FETs family, monitoring the gate-control on the drain current. The drain current is activated by the V_{DS} voltage under tunneling conditions. But the gate terminal modulates the carriers concentration and consequently the drain current flow, accordingly with its inherent included SOI structure. Also, a new model parameter comes to complete the NOI theory. The third order derivative was used for the extraction of a threshold drain-source voltage that splits the work domain in two conduction regions.

Keywords: SOI devices, Field Effect Transistors, modeling, simulation.

1. Introduction

The NOI nanotransistor architecture was inspired from a real sub-10 nm undulated poly-silicon film that produced a special SOI device, [1–3].

The structure was firstly modified as a SOI-MOSFET nanotransistor, with a thinner film in the device body, [4]. In this way, two 7 nm thickness n-wells, representing the source and drain regions, were connected by a 1 nm thickness p-type semiconductor, representing the transistor body. This middle film can be thinned up to few

atomic layers, achieving a limit SOI structure, [5]. In these devices with a cavity above the transistor body, the conduction between Source and Drain occurs through the solid-state ultra-thin p-type body – as a MOS current and through vacuum – as a tunnel current. The next step is the completely removing of the middle layer, obtaining "*Nothing On Insulator*" transistor that was firstly proposed, due to its relationships with SOI devices, [6–10]. The "NOI" acronym was elected as a mirror term to the "SON" acronym – Silicon On Nothing, [11]. Now the "Nothing" region ensures the entire Source-Drain conduction, via the tunnel current, being the NOI nanotransistor *body*, Fig. 1.

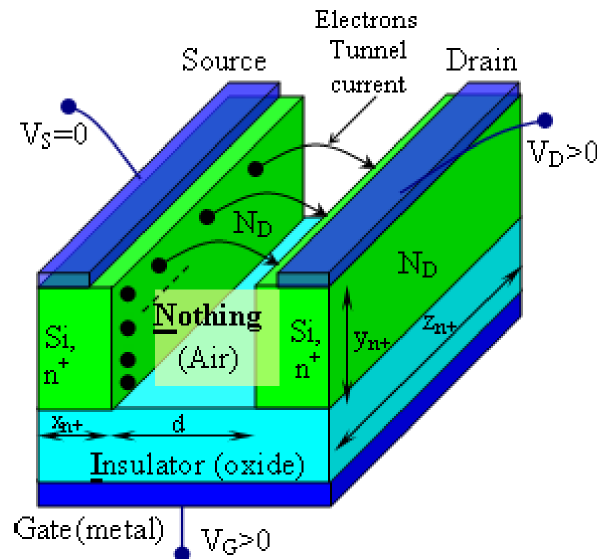


Fig.1. The NOI nanostructure with the explicit x_{n+}, y_{n+}, z_{n+}, d notations.

2. Analytical model for I_D–V_{DS}

The starting sizes for the Si-n$^+$ well were unrealistic in a prior study, [12, 13]. Therefore, the actual Si islands sizes are risen, but maintained sub-10 nm: $x_{n+} = 3$ nm, $y_{n+} = 10$ nm, $z_{n+} = 10$ nm and d = 3 nm. The doping concentration, N_D was also increased up to $5{\times}10^{20}$cm^{-3} that means *150 impurities* / n$^+$– island volume. The maximum depleted film width in the Si-n$^+$ regions is $\sim$ 2 nm, [14]. So, the source and drain regions with 10 nm Si-structure are SOI partially-depleted structures with clear limit conditions.

The current flow on the longitudinal direction, I_D is ensured by the Drain-Source voltage, V_{DS}. Due to the electrons tunneling through a triangle potential barrier with the height equal with the electrons affinity from semiconductor to vacuum, χ_s, the drain current is:

$$I_D\left(V_{DS}\right) = A \cdot V_{dsT} V_{DS} \cdot \exp\left(-\frac{B}{V_{DS}}\right) \quad (1)$$

where A, B are constants depending on χ_s and geometrical sizes of NOI-FET, [12], V_{DS} is the drain-source voltage and V_{dsT} is a constant model parameter, named threshold drain-source voltage. The proposed model (1) is an approximation of a physical model, previously presented, [12].

The new model (1) is acceptable in the V_{dsT} vicinity. The target of the approximated model (1) is to offer a function with oblique asymptotes.

The simulated output characteristics, $I_D - V_{DS}$, at $V_{GS} = 0.6$ V and $V_{GS} = 1$ V, seam to present a sub-threshold conduction for $V_{DS} < 4$ V, Fig. 2, black curves. Here, the NOI-FET transistor seems to present a drain-source threshold voltage.

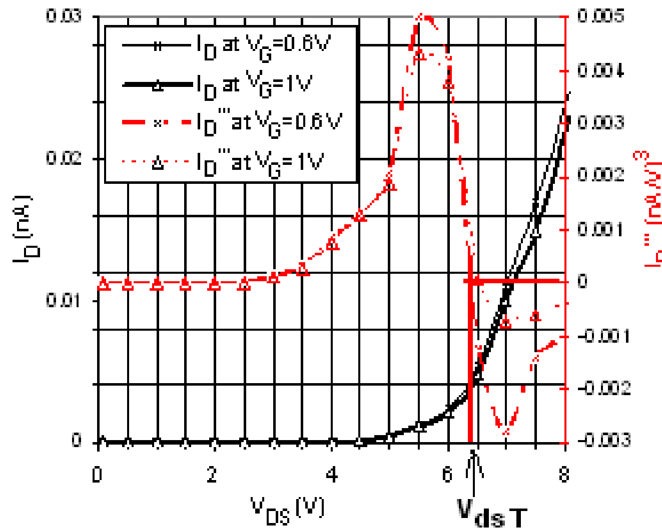


Fig. 2. The simulated characteristics for the NOI-FET, V_G= 0.6 V and 1 V in black lines at the left side and the third order derivative values in the right side.

A valuable tool in order to characterize a non-linear conduction and to extract an accurate threshold point is the *Non-Linear Electrical Conduction Theorem NECT*, [6]. Accordingly with this theorem: for any nonlinear electrical conduction function with asymptotic behaviors at $\pm\infty$, there is at least, a point where the third order derivative gets zero value. The zeroing values have a "threshold" value meaning.

The threshold voltage V_{dsT} can be extracted now by numerical derivative of the simulated $I_D - V_{DS}$ curves by Origin, Fig. 2, curves in red. The value $V_{dsT} \approx 6.4$ V results from the I_D''' interception with the horizontal axis. This parameter is a starting point in the device comprehension and represents a certain boundary between a weak and strong conduction for the $I_D - V_{DS}$ characteristics.

3.The carriers concentration dependence on V_{GS}

The goal of this paragraph is to solve the Poisson's equation in non-depletion approximation for the n$^+$-film. In a previous work, the Poisson equation was integrated for a 50 nm SOI film, in the depletion approximation, [15]. The analytical argument for the NOI structure affiliation to the FETs class results from the sensitivity in trans-conductance terms.

The energetic diagram from the Fig. 3 is associated with the Source / n$^+$-Island (film) / Oxide support / Gate segment of structure. The notations are: E_F – the Fermi level energy in film, E_i – the middle energy in the forbidden band that is the reference level in the neutral n$^+$-film, Φ_F – the Fermi potential, V_S/V_G – the applied Source/Gate biases, V – is the potential at x coordinate, $\beta = q/(k\mathrm{T})$ – the reverse thermal voltage, x – the spatial coordinate, $\varepsilon_{Si/ox}$– the dielectric permittivity of Si/oxide, q – the elementary electrical charge, n_i – the intrinsic carriers concentration. The Poisson's equation in film can be written as:

$$\frac{d^2V}{dx^2} = -\frac{qn_i}{\varepsilon_{si}}\left[\, e^{-\beta(V+\Phi_F)} - e^{\beta(V+\Phi_F)} + e^{\beta\Phi_F}\,\right]. \tag{2}$$

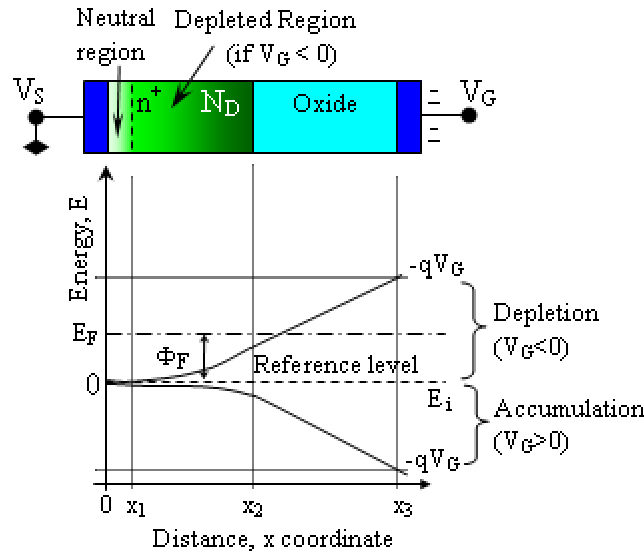


Fig. 3. Energetic diagram for the n$^+$-film on Oxide.

Considering the variable changing: $-\mathcal{E} = \mathrm{d}V/\mathrm{d}x$, where $\mathcal{E}$ is the electric field. The general solution yields after a first integration. The limit conditions $\mathcal{E}(0) = 0$, $V(0) = V_S = 0$ provide the electric field expressions versus the film potential V.

Because the oxide doesn't contain electrical charges in this analysis, a constant value of the electric field in oxide occurs. From the conservation of the normal electric induction component at $x = x_2$, $\varepsilon_{Si} \cdot \mathcal{E}_{Si}(x_2) = \varepsilon_{ox}\mathcal{E}_{ox}(x_2)$ and replacing the electric

field from Si at $x = x_2$, a specific relationship between V_G and f_S is obtained for $V_S = 0$:

$$V_G = f_S + \frac{x_{ox}}{\varepsilon_{ox}} \sqrt{\frac{2\varepsilon_{si} q N_D}{\beta}} \left[\left(e^{-\beta f_S} - 1\right) \cdot \frac{n_i^2}{N_D^2} + \left(e^{\beta f_S} - 1\right) - \beta f_S \right]^{1/2}, \quad (3)$$

where $V(x_2)$ was notated by f_S and x_{ox} is the oxide thickness, N_D is doping concentration.

For a higher positive V_G, a higher f_S results and a higher electrons accumulation occurs:

$$n = n_i \cdot \left[e^{\beta(f_S + \Phi_F)} \right]. \quad (4)$$

The electrons charge elevation in the n$^+$-island represents a higher electric charge reservoir available for tunneling. Hence, this theoretical approach proves the carriers charge modulation by the gate-voltage V_G, as in the FETs cases.

Figure 4 presents the $f_S(V_G)$ dependence for $x_{ox} = 100$ nm and different doping concentrations.

Obviously, a thinner oxide support provides a larger range for f_S when V_G varies. From the transconductance point of view a thinner oxide is preferable, but from the breakdown point of view its thickness must by increased up to 100 nm.

Figure 4 reveals also another aspect: a higher doping concentration in the n$^+$-film is a deceptive selection. If $N_D = 2 \times 10^{21}$ cm^{-3}, that means $\sim$ 800 electrons / n$^+$-film available for tunneling, seams to be more comfortable instead $\sim$ 150 electrons if $N_D = 5 \times 10^{20}$ cm^{-3}. But this is true only at $V_G = 0$ V. The accumulation process becomes more sensitive with the gate voltage at lower doping concentrations, Fig. 4.

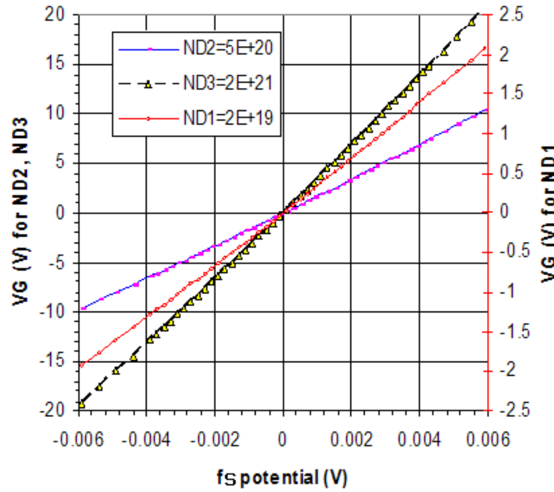
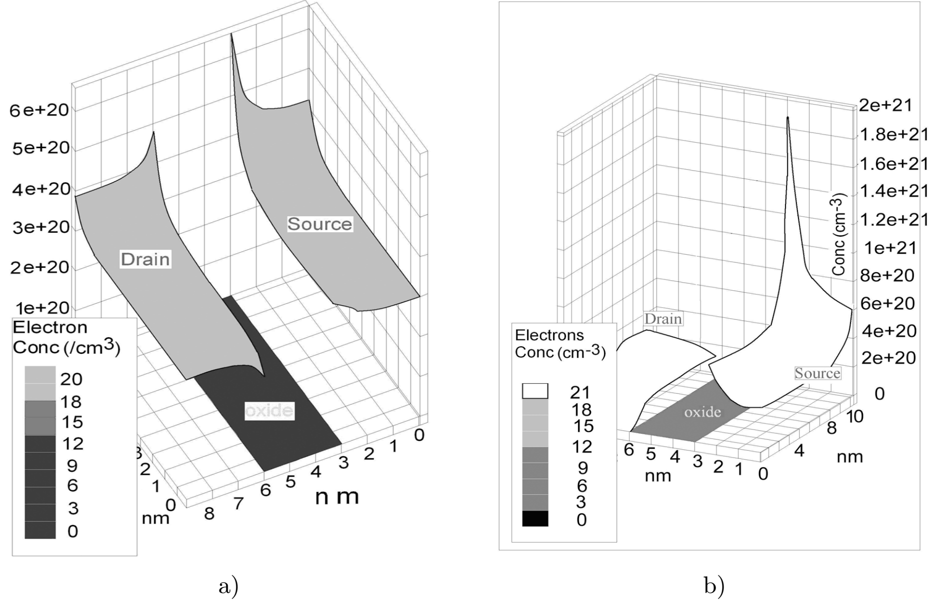


Fig. 4. The $f_S - V_G$ dependence at distinct N_D.

4. Simulations results

Usually the simulations help for a macro-model establishing, [16–19]. The analytical models are completed with Atlas simulations to emphasize the gate and drain control on the I_D current. These voltages produce a non-uniform electrons concentration in the source and drain n^+-films.



a) b)

Fig. 5. Electrons concentration in the source and drain region at: (a) $V_{DS} = 0.3$ V and $V_{GS} = 3$ V; (b) $V_{DS} = 4$ V and $V_{GS} = 5$ V.

Both for Fig. 5 and Fig. 6, the simulated NOI-FET structure has the architecture like in Fig. 1 and the parameters from Section 2: $x_{n+} = 3$ nm, $y_{n+} = 10$ nm, $z_{n+} = = 10$ nm, $d = 3$ nm, $x_{ox} = 100$ nm and $N_D = 5 \times 10^{20}$ cm^{-3}. Figure 5a presents the electrons concentration in the source and drain regions, at $V_S = 0$ V, $V_D = 0.3$ V, $V_G = = 3$ V. The maximum value $n = 7 \times 10^{20}$ cm^{-3} corresponds to an accumulation regime. The drain currents $I_D = I_S = 10^{-17}$ A show a weak conduction and $I_G = 4 \times 10^{-25}$ A ensure the breakdown avoiding. In Fig. 5b the maximum electrons concentration reaches $n = 2 \times 10^{21}$ cm^{-3} in the Source region and $n = 4 \times 10^{20}$cm^{-3} in the Drain region at $V_S = 0$ V, $V_D = 4$ V, $V_G = 5$ V, for the same structure. Hence, the average electrons concentration is: 2.2×10^{20} cm^{-3}, respectively 3.8×10^{20} cm^{-3}, for Fig. 5a, Fig. 5b, in a good agreement with the analytical model (4).

Figure 6 presents the Drain and Gate currents versus the applied Gate voltage at $V_{DS} = 4$ V. The currents proofs a leakage current through the gate terminal, low enough to consider that the breakdown is still avoided.

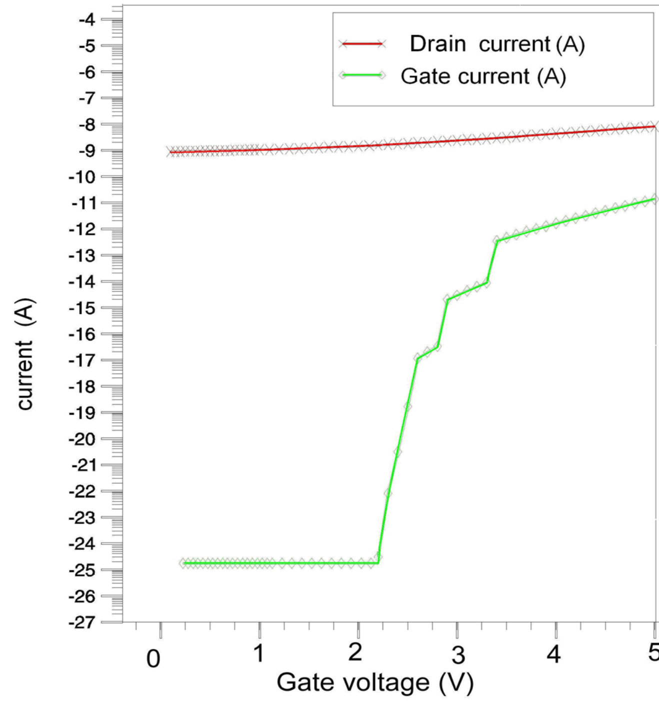


Fig. 6. For 100 nm oxide thickness NOI structure, the currents I_D rises with V_G rising, while I_G preserve a leakage value ($I_G = 10^{-24}$ A...1 pA << I_D = 1...8 nA).

5. Conclusions

The paper presented some theoretical aspects of a new nanostructure derived from SOI: Nothing On Insulator and brought two arguments in order to demonstrate the NOI device affiliation to the Field Effect Transistors class.

The developed analytical model offers for any others sizes and doping concentrations the potential f_S versus the applied V_G voltage, in all the regimes: accumulation, depletion and inversion. The curves from Fig. 4 represent an analysis example, for NOI structure designing to achieve the maximum variation for the f_S potential at a given V_G variation. In this way, the electrical charge variation at an incident gate stimulus is maximized besides to the drain current range.

The theoretical model was accompanied by numerical simulations of a NOI nanostructure in order to present an optimum transconductance and to avoid the insulator support breakdown.

A new threshold parameter, V_{dsT}, numerically extracted by the third order derivative zeroing, highlights a non-linear conduction – specific for the active devices, as FETs.

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