

A Flexible Fabrication Process for RF MEMS Devices

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Abstract. RF MEMS are assuming a great importance in the fast evolving telecommunication market and space applications. In the last years a flexible technology platform has been developed and continuously optimized at FBK (Italy) for the fabrication of RF MEMS basic components as well as complex RF circuits working in the frequency range from sub-GHz up to more than 100 GHz. The paper reports about the fabrication process and its capabilities. The most important process features are described together with some modifications required for the manufacturing of specific devices, like dielectric less RF MEMS switches. Examples of produced devices and their performances are briefly presented.

Keywords: RF-MEMS, fabrication process.

1. Introduction

RF MEMS are assuming a great importance in many fields, like the fast evolving telecommunication market and space applications. Many advantages are reported with respect to components in standard technology, like small dimension, high performance, low manufacturing cost and low power consumption [1].

In the last years a flexible technology platform has been developed and continuously optimized at FBK (Italy) for the fabrication of RF MEMS basic components (like ohmic and capacitive switches, variable capacitors and inductors), as well as

complex RF circuits working in the frequency range from sub-GHz up to more than 100 GHz.

Using the base 8-lithography mask process and some expansion modules tailored for specific requirements, many devices for both space and communications applications have been produced. Some typical examples are switching matrices, redundancy switches, tunable filters, tunable and switchable phase shifter, reconfigurable antennas and impedance matching networks. In this paper the basic process, some of its extension modules and a few results are presented in detail.

2. Process features

The fabrication process was developed to produce complex circuits including MEMS switches and passive components on high resistivity silicon wafers. Low losses gold coplanar waveguides (CPWs) and microstrip lines are requested for the transmission of RF signals, while high resistivity DC bias lines and electrodes are used for switch actuation in order to reduce RF losses. RF and DC signals have to be separated and high isolation is requested between DC actuation electrodes and movable bridges to avoid breakdown at voltages up to 100 V. Capacitive switches require high capacitance in the actuated position, therefore a thin dielectric is needed over RF signal line and floating metal electrodes are required to have a repeatable capacitance, reducing the negative effects due to membrane deformations induced by stress. Ohmic contacts require low contact resistance and therefore the contact materials, position, and force have to be reliable and well controlled.

3. Base process flow

A scheme of the process flow is reported in Fig. 1. The fabrication process starts with the realization of an insulating layer consisting of 1 μm of silicon oxide grown by wet thermal oxidation at 975°C. The charges trapped at the silicon-oxide interface can induce a conductive channel that increases the losses on the substrate by capacitive coupling; an annealing at 975°C for 50 min in nitrogen atmosphere is performed in order to reduce them. A 630 nm thick layer of polysilicon is then deposited by Low Pressure chemical Vapour Deposition (LPCVD) at 630°C (Fig. 1a).

The polysilicon layer is then ion implanted using boron ions (BF₂) at 120 keV. The dose can be adapted depending on the required resistivity. Typically 6.2×10^{14} B/cm² is used to obtain a sheet resistance of about 1600 Ohm/sq. With the first lithography step the polysilicon biasing line and actuation electrodes are defined and then dry etched by Cl based chemistry in a Tegal 6510 dual chamber dry etcher. To improve the contact resistance small dimples (4×4 μm) of polysilicon are realized to define exactly the number and position of contact points between the movable membrane and the underpass signal line. After removing the photoresist layer, the implanted B ions are diffused and electrically activated by an annealing at 925°C for 1 hour in nitrogen atmosphere to obtain the required doping profile. A 300 nm thick insulating layer of SiO₂ is deposited by LPCVD (Low Pressure Chemical Vapour Deposition)

using TEOS (Tetraethyl orthosilicate) at 718°C. A second lithography step and a dry etching (using F based chemistry in a Tegal 903 etcher) define the opening for the contacts (Fig. 1a).

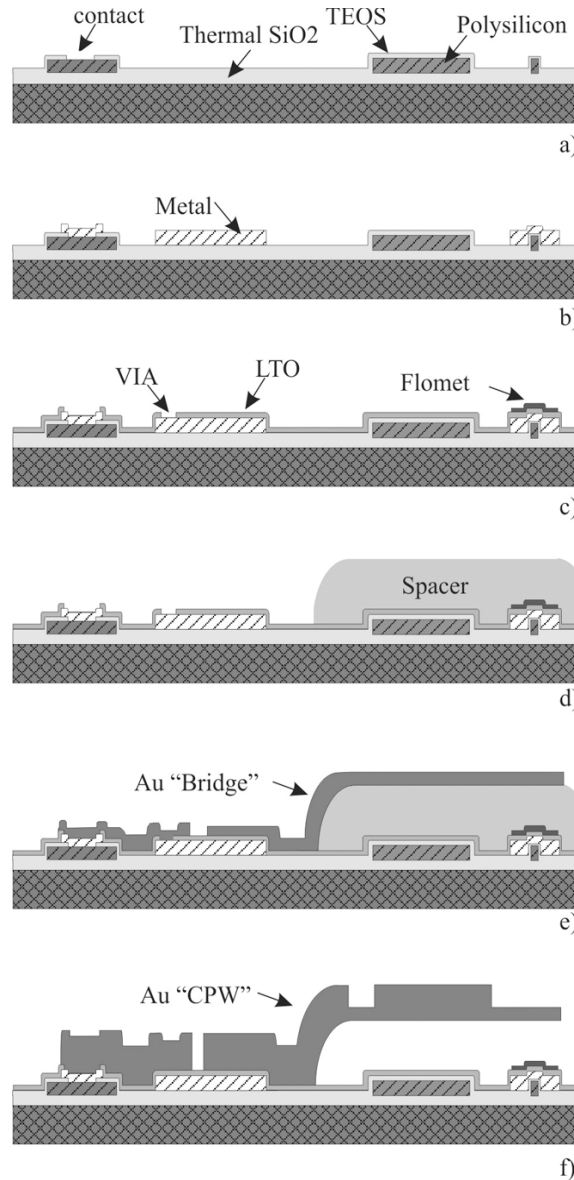


Fig. 1. Process flow: a) thermal oxidation; polysilicon and TEOS deposition and contact opening; b) metal deposition and patterning; c) LTO deposition, vias opening and floating metal deposition; d) spacer deposition and backing; e) seed layer and first Au "Bridge" electroplating; f) second Au "CPW" electroplating and release of suspended structures.

A conductive metal layer (Al 1%Si) is then deposited by sputtering. A diffusion barrier (Ti/TiN) is used to avoid spiking at the polysilicon interface and hillocks formation on the top. The resulting multilayer is composed of 30 nm Ti, 50 nm TiN, 410 nm Al 1%Si, 60 nm Ti and 80 nm TiN. The thickness of the multimetal underpass and the polysilicon actuation electrodes has to be the same in order to avoid distortions in the actuated bridge. The metal is defined by the third lithography and dry etched in the TEGAL 6510 (Fig. 1b). A 100 nm thick SiO₂ dielectric layer (Low Temperature Oxide LTO) is deposited by LPCVD at 430°C using silane. The fourth lithography step defines the vias in the LTO that are dry etched in the TEGAL 903 (Fig. 1c). A 5 nm Cr 150 nm Au layer is deposited by electron beam gun to be used both as electrically floating metal layer over capacitors and to reduce the metal-Au resistance inside vias. The Cr is used as adhesion layer because gold has a very poor adhesion over silicon oxide. The floating metal is defined by the fifth lithography step and wet etched (Fig. 1c). Photoresist (HiPR 6517HC from FujiFilm) was chosen as sacrificial layer (spacer) for the fabrication of suspended movable membranes and air bridges, because it can be easily removed by oxygen plasma. The drawback is that only a partial planarization is obtained. The standard thickness is 3 μm but, depending on device requirements, different thicknesses are used ranging from 1.6 to 4.5 μm. After the sixth lithography to define the spacer, the resist is backed at 200°C, a temperature much higher than the usual one, in order to round the edges to improve step coverage, as well as to increase the photoresist chemical and mechanical resistance (Fig. 1d). After this treatment the resist is not dissolved by the solvents used in the next steps and, further lithography steps can be performed without damaging the spacer.

A conductive seed layer for the electroplating process is then evaporated all over the wafer. This layer is composed of 2.5 nm of Cr, for adhesion to substrate, 25 nm of Au as conductive layer and a sacrificial top layer of 2 nm of Cr, to increase the adhesion of the photoresist mask during electroplating. In the seventh lithography step the pattern of the first Au film is defined by using a 6 μm thick layer of AZ 4562 positive resist (from AZ-Electronic Materials). After wet etching of the top Cr layer, 1.8 μm thick Au layer, the so-called “Bridge” layer, is electroplated by using cyanide based chemistry (Auroloyte CN 200 by Atotech) (Fig. 1e). The deposition parameters have been chosen in order to obtain a slightly tensile residual stress. After photoresist removal, the eighth lithography step defines the pattern of a second thicker (3.5 μm) Au layer called “CPW”, which is also grown by electroplating. The thinner “Bridge” layer is used mainly to fabricate the suspended and movable structures while low resistance lines, ground areas and the anchor points of movable structures are fabricated by superimposing both the gold layers. Frequently the “CPW” layer is deposited over selected areas of movable bridges in order to have stiffer parts that move rigidly while deformation is localized on thinner suspension spring legs. In order to control the contact force on ohmic switches the central part of the movable membrane is made of a thick (“Bridge” plus “CPW”) Au layer, so that it moves rigidly over the actuation electrodes. Cantilevers tips or lateral wings on clamped-clamped beams are designed using only thinner “Bridge” layer, so that they can bend up and contact the signal line over polysilicon dimples (Fig. 2). In this way the contact force

is defined by the amount of deflection (dimple height) and the elasticity of wings.

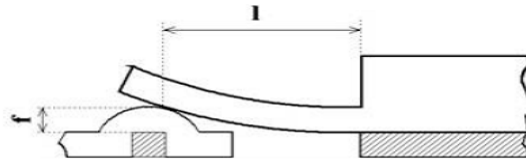


Fig. 2. Scheme of ohmic contact with polysilicon dimple and thin flexible cantilever tip.

The seed layer is removed by wet etching and a gold sintering at 190°C is performed to increase the gold adhesion to substrate and the bondability of pads for external connections. In addition this step leads to a more homogeneous and reproducible (tensile) stress value in the gold membranes. The last process step is the release of suspended structures by removal of sacrificial resist with oxygen plasma (Fig. 1f). The process temperature and the etching parameters were optimized in order to reduce the structure deformations induced by stress and stress gradient along the thickness of films [2].

4. Process modifications

The 8-mask base version of the process, was modified to adapt to specific applications, increasing the number of lithography steps. A backside metallization has been added, either sputtered aluminum or electroplated gold, to realize microstrip lines, antennas and other devices on the wafer backside. To realize calibrated resistors and to reduce the polysilicon – metal contact resistance a second B ion implantation of polysilicon has been added, using photoresist as masking layer. By using TMAH anisotropic etching, the Si substrate has been locally removed to realize devices like inductors and interdigitated capacitors on very thin suspended dielectric membrane [3], or to realize through-wafer vias in order to electrically connect front and backside of the wafer.

To reduce substrate losses at high frequency (up to 200 GHz) quartz substrates has been used. To process the transparent substrates in some equipments it was requested to deposit and then remove an opaque sacrificial layer on the backside (either sputtered Al or PECVD amorphous polysilicon).

This RF Switch technology has also been integrated on different substrates (*e.g.* GaN, SOI) by post-processing wafers with active devices already fabricated.

A critical issue of capacitive switches is dielectric charging; a recent improvement of design allows dielectric-free electrodes switches to be realized using the same process. Both TEOS and LTO oxide have been removed over the polysilicon actuation electrodes by increasing the over etching time during the vias opening. To avoid short circuits a matrix of mechanical stoppers (Fig. 3) has been distributed over the electrodes surface in order to obtain an air gap of about 550 nm between movable bridges and biasing electrodes, thick enough for isolation at the voltage normally used. With

this solution the shift of actuation voltage induced by dielectric charging is drastically reduced. During short cycling test, switches with dielectric actuates at about 60 V the first time, at about 70 V the second time and then at slightly increasing voltage up to stabilization after 10, 15 cycles. Dielectric less switches with the same geometry show negligible modification of the actuation voltage. On long term continuous voltage stress characterization [4] only small voltage shift were reported after 8 hours, as reported in Fig. 4.

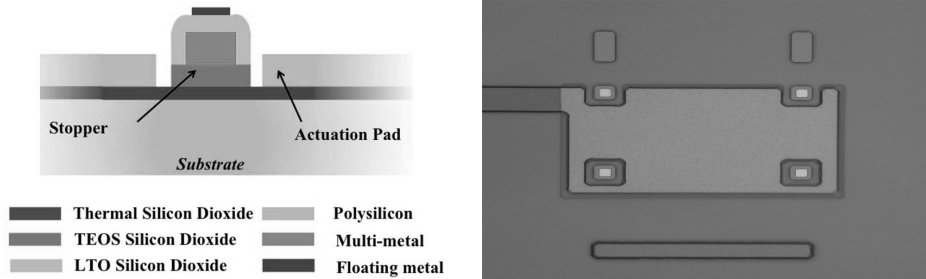


Fig. 3. Scheme of pillars used as stoppers in dielectric free actuation electrodes and picture of a polysilicon actuation electrode with pillars.

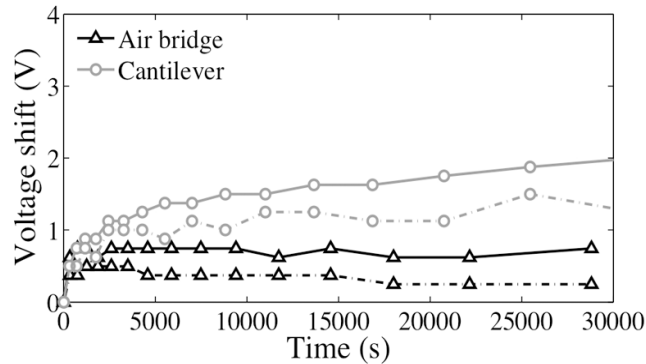


Fig. 4. Pull in (continuous line) and Pull out (dashed line) voltage shift for air bridge and cantilever switches during long term continuous voltage stress.

5. Process results

Many devices have been produced using either the base process or its modifications, starting from both capacitive and ohmic single switches to complex circuits. Switches gave good results in terms of RF performances. Series Ohmic switches give good isolation, particularly in the range from 0 to about 10 GHz, and low insertion loss. At higher frequency the isolation is reduced by the effect of the residual capacitance of the switch in the up position. The cantilever switch reported in Fig. 5 exhibits isolation better than 20 dB and insertion loss lower than 0.3 dB for frequency up to 30 GHz.

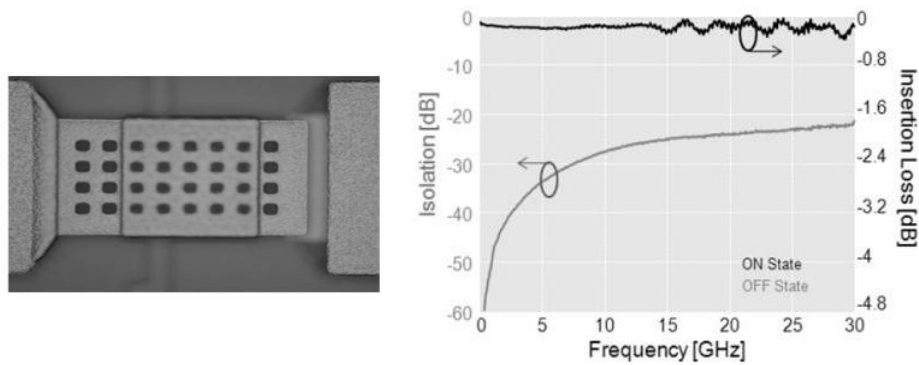


Fig. 5. Cantilever Ohmic switch.

At high frequencies, capacitive shunt switches are more appropriate. They give a good isolation in a defined frequency range that can be tailored for the device requirements as a function of the switch capacitance and parasitic inductance. Capacitive switches working at frequency up to 200 GHz were realized.

By using the “Boosted” configuration [5] it is possible to obtain a high on/off capacitance ratio. The capacitance in the actuated state is defined by the area of the MIM capacitor constituted by the Metal underpass, the LTO Insulating layer and the electrically floating Metal upper electrode. Designing the movable bridge in order that only narrow lines will contact the floating metal it is possible to minimize the capacitance in the up position. The capacitive shunt switch presented in Fig. 6 was designed for a central frequency of 27 GHz. the capacitance in down position is 4.55 pF, while in up position it is only 21 fF giving a ratio of 215. Higher ratios can be easily obtained by increasing the MIM capacitor area.

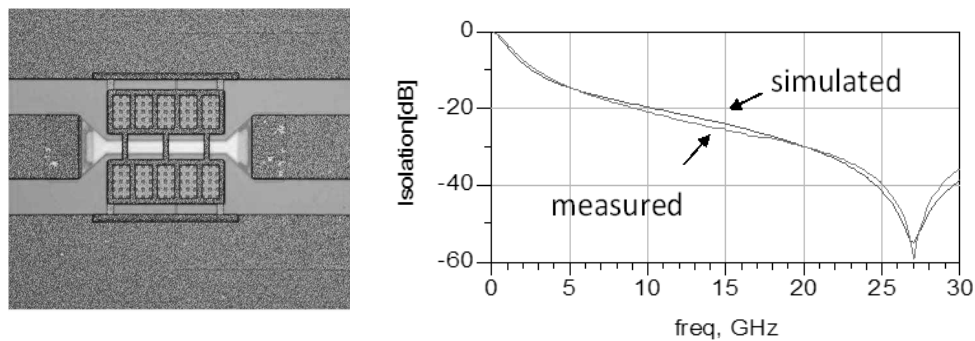


Fig. 6. Capacitive shunt switch.

By using both ohmic and capacitive switches it is possible to obtain high isolation over a higher frequency range. On the SPDT reported in Fig. 7 it was used for each branch a series ohmic and a capacitive shunt switch. A strong increase of the isolation is obtained by actuating the shunt switch [6]. The loss was less than 1 dB

up to 30 GHz with a maximum of about 1.5 dB at 40 GHz. These components were used to fabricate 2×2 switching matrices (Fig. 8), a building block for more complex switching matrices for space application.

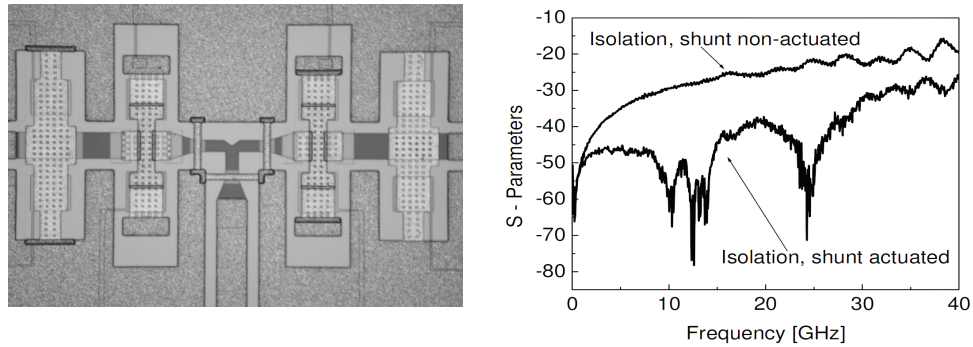


Fig. 7. Picture and isolation parameters of SPDT switch using both series and shunt switches to increase isolation at higher frequency.

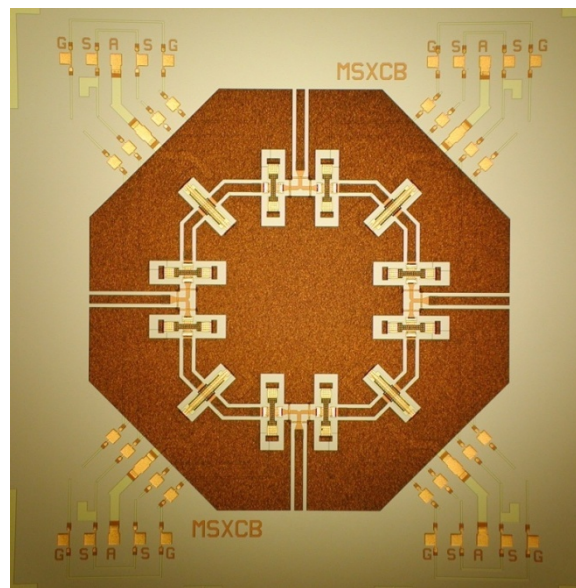


Fig. 8. 2×2 switching matrix using both series and shunt switches.

Using the switches in combination with other passive elements more complex devices were fabricated like 0 to 360° 5 bit phase shifter [7] (Fig. 9) or switchable band pass filter with capacitors and inductors suspended on thin dielectric membrane [3] (Fig. 10).

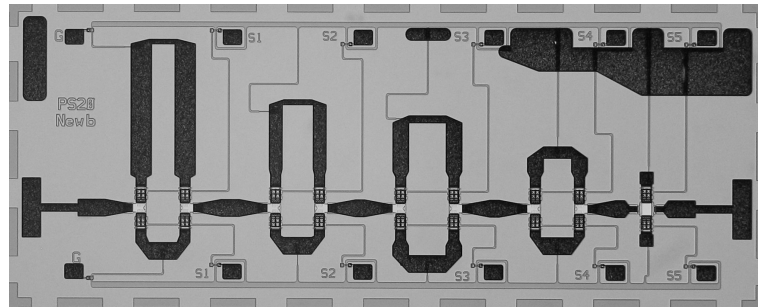


Fig. 9. 5 bit phase shifter.

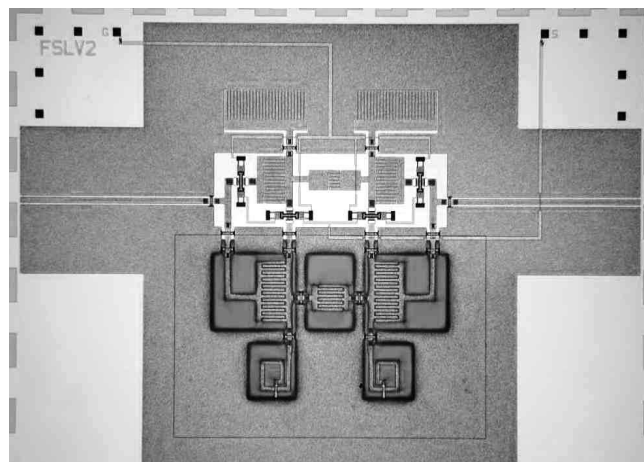


Fig. 10. Switchable 1.8–5.2 GHz filter with capacitors and inductors on suspended dielectric membrane.

6. Conclusions

The paper reports about the fabrication process for RF MEMS devices developed at FBK. The basic features of the process are outlined and the whole process flow is described in detail. Special attention is dedicated to the implementation of additional process modules that respond to specific devices requirements. Finally a selected number of realized devices and their performances are presented.

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