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Operating Frequency Extension of Surface Assembled Microwave Components

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Abstract. A novel transition from microstrip and coplanar lines to the specific signal interfaces of usual surface assembled components is considered in this paper. It is aimed to improve the bandwidth of printed circuit board (PCB) based packages, provided by smaller values and better geometry controlled parasitic elements due to proposed structure. Moreover, the same interface model is compatible with surface assembly of substrate integrated waveguide components. Guidelines for component values preliminary calculation and optimization are presented. Microstrip test circuits were accordingly manufactured for design verification, with satisfactory results up to 8 GHz. The relative permittivity of FR-4 substrate material used in our experiments is considered the solely responsible for certain differences existing between simulated and experimental data, because they became effective after PCB manufacturer was replaced.

Keywords: surface mount assembly, coplanar waveguide, microstrip line, low-pass filter, substrate-integrated waveguide.

1. Introduction

Microwave communication systems require a certain flexibility regarding critical components assembly, mainly filters or diplexers, in order to cope with changing radio regulatory requirements within different geographical areas. Component manufacturers need low cost and reliable technical solutions for solving this hard to deal problem, especially for very high frequency applications.

The working bandwidth of a surface assembled component is inherently limited by parasitic elements associated with connection interface elements, because their

frequency response depends on geometrical dimensions of all structure constituent parts. This explains why micro-leadframe package (MLP) presented in Fig. 1a [1] can be used up to 20 GHz in case of an air filled internal cavity, hermetically sealed with a ceramic or plastic lid [2]: pad areas are very small (usually between 0.2–0.5 mm^2), and the pad pitch ranges from 0.5 to 1 mm (0.65 mm in Fig.1.b example), due to special technologies involved in package manufacturing and internal device assembly techniques. Unfortunately, in order to keep reasonable production costs, MLPs are exclusively used for *small area* semiconductor devices.

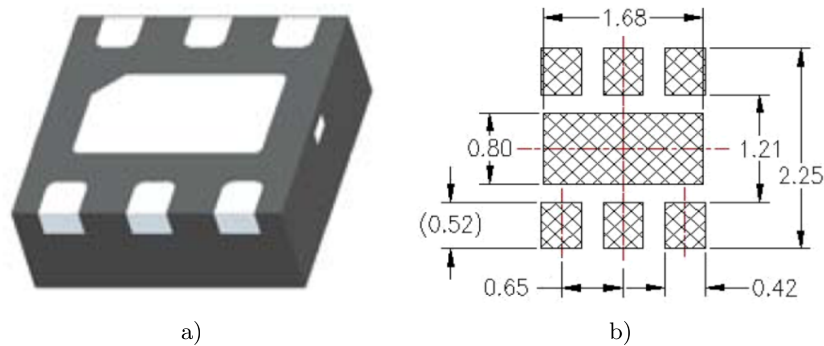

Fig. 1. MLP package: (a) bottom view;
(b) corresponding footprint. All dimensions in [mm].

Different solutions, like cost effective printed circuit board based packages (Fig. 2 presents a simple model and the prescribed footprint [3]), are available for larger circuits and components. They are normally used up to maximum 5–7 GHz working frequency, since the footprint dimensions lead to higher values of related parasitic elements.

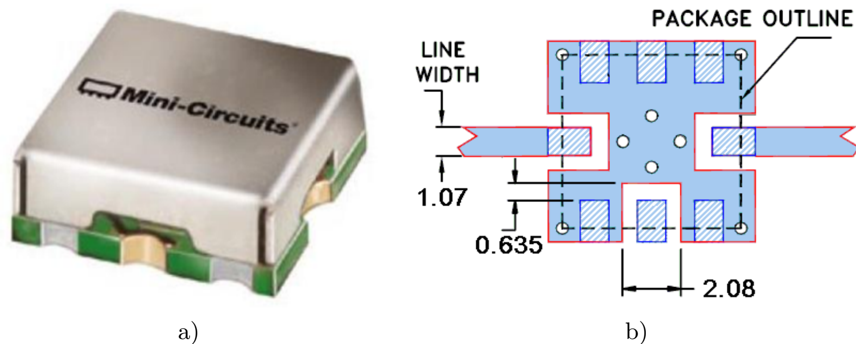

Fig.2. PCB-based package: (a) component view; (b) recommended footprint.

Increased pad dimensions defined on the main printed circuit board (PCB) compared with associated component pads result from assembly reliability considerations, therefore prevailing over maximum available working frequency customary observed on most of PCB-based packages and components:

- it is mandatory to have enough guard space due to expected positioning errors during placement and soldering processes;
- the vertical metal layer connected with each pad (as shown in Fig. 2a) helps creating a soldering alloy meniscus in the area where the metal surfaces are bonded, thus contributing to the improvement of local mechanical strength;
- a well soldered component withstands thermal and mechanical stresses in a better way.

The paper presents a new approach for surface mounting assembly of planar transmission line based packages by utilizing a specific transition model. from microstrip and coplanar lines miniature coaxial connectors to SIW structures [9], which can be adapted as a general component connection mechanism, more flexible regarding the transmission line interfaces intended to form a junction, compared with presently used types. The new transition can be tested from reliability point of view, mainly for stand-alone SIW components used in lower frequency applications. A compatible transition to microstrip transmission line is also proposed, in order to improve the assembly flexibility during product life cycle; small adjustments may be required for different substrate heights.

2. Connection equivalent circuit and frequency response

RF port matching for any SMD package is usually guaranteed by component manufacturers within a certain bandwidth, for the assigned footprint configuration (all signal and ground pads) and well defined thickness and permittivity of the main assembly board. Because this footprint acts like an optimum interface, severe deviations of its characteristics could affect the component or system operation, *e.g.* nonuniform frequency response, distortions or stability issues.

The parasitic elements normally associated with RF and ground pad connections can not more be neglected at very high frequencies due to physical considerations, therefore it is really important to maintain them to *well controlled values*, according to specific microwave impedance matching rules. This is possible by creating equivalent circuits intended to describe their electrical behavior in a certain frequency range. The usual lumped element equivalent circuit (Fig. 3a) is of low-pass filter (LPF) type, aimed to absorb the following components:

a) a series inductor associated with existing series element(s) between surface assembled component and the base PCB (this equivalence is also valid for any via hole, including the grounding ones);

b) two grounded shunt capacitors, corresponding with the discontinuities created by open ended transmission line (TL) or other similar elements and transitions from pads to the feeding TL.

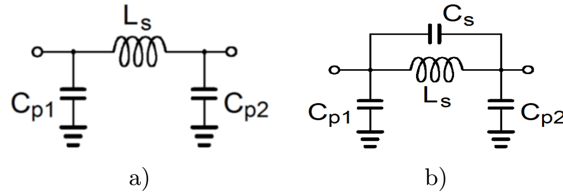

Fig. 3. Equivalent circuit of a pad-to-pad connection:
(a) regular LPF cell; (b) with additional element C_s.

This straightforward LPF model may be expanded with additional components, if the field distributions ask for such behavioral equivalence; *e.g.* C_s in Fig. 3b was included in order to take into account a certain fringing capacitance at very high frequency. A symmetrical configuration ($C_{p1} = C_{p2}$) is advisable in most cases for similar generator and source impedances, due to impedance transforming properties of any two-port containing reactive elements. Considering the frequency response parameters (both matching and transfer characteristics) of these structures, there are some configuration constraints and selection criteria for the circuit designer:

- ultra-broadband or narrowband impedance matching;
- correlation between relevant microwave requirements and the interfaces' mechanical or technological mandatory limits;
- other layout restrictions;
- reliability and implementation costs vs. customer demands.

2.1. Series inductor calculation

The first component on which we turn our attention in Fig. 3 is the series inductor L_S because its inductance is mainly determined by geometrical factors and also unlikely to be adjusted, as results from certain manufacturing constraints. In addition, the corresponding reactance modulus is directly proportional with calculation frequency f:

$$X_{L_S} = 2\pi f L_S, \tag{1}$$

hence the signal transmission will worsen as frequency increases due to poorer impedance matching and higher attenuation, if proper capacitive compensation elements are not used as parts of a well designed LPF. Consequently, frequency performance optimization of this filter which describes the simplest component connection has to start with inductance calculation.

The equivalent inductance of complex physical configurations can usually be obtained with excellent accuracy by numerical methods. However, good enough tolerance can be obtained with simple analytical formulas, useful as first order approximation for the maximum working frequency limit. Ref. [6] offers the following relation for the self-inductance of a straight metal wire, expressed in [μH]:

$$L_S = 0.002\, l \left[\ln\left(\frac{4l}{d}\right) - 1 + \frac{d}{2l} + \frac{\mu_r T(x)}{4} \right], \tag{2}$$

where

$$T(x) = \sqrt{\frac{0.873011 + 0.00186128x}{1 - 0.278381x + 0.127964x^2}} \tag{3}$$

adds a correction for high frequency effects and the parameter x is defined as:

$$x = \pi d \sqrt{\frac{2\mu f}{\sigma}}. \tag{4}$$

Other terms in the above expressions are:
d = external diameter of the wire [cm],
l = wire length [cm],
f = working frequency [Hz],
μ = metal wire permeability [H/m],
μ_r = metal wire relative permeability,
σ = metal wire conductivity [S/m].

2.2. Low-Pass filter response optimization

The component values of a LPF structure intended for a broadband application are usually designed to provide a very good input impedance matching over the whole required bandwidth, which results in optimum signal power transfer from the source to the load. This task can be accomplished in case of most design constraints with high performance software applications for linear circuit analysis and optimization. Because the equivalent circuits in Fig. 3 are used to describe the broadband behavior of a surface assembled component connection having the inductance value already determined as presented in the previous section, the designer needs also information about maximum attainable bandwidth for this inductance and the calculation of corresponding capacitance values.

The results of a sample calculation are presented in Fig. 4, obtained by circuit optimization procedure using [4] with the best impedance matching target. Both circuits shown in Fig. 3 were analyzed for the same likely 0.5 nH series inductance, with the calculated component values listed in Table 1. The return loss curve corresponding to the solely L_S inductance is supplied too, so that presented graphs allow easier comparison of all possible circumstances.

Table 1. Optimization results

Configuration	L_S **[nH]**	$C_{p1} = C_{p2}$ **[pF]**	C_s **[pF]**
Fig. 3a	0.5	0.1135	–
Fig. 3b	0.5	0.12	0.055

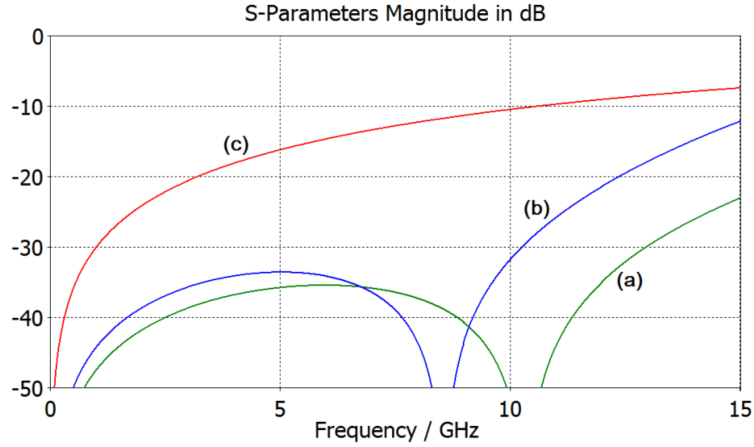

Fig. 4. Input return loss calculated for (a) standard LPF cell; (b) expanded LPF; (c) L_S series inductor only.

Capacitance values in Table 1 are the *necessary* condition regarding the best wide-band return loss availability, until complete layout analysis *proves* their achievement. This means that the optimization process alone is not yet relevant, because the real connection structure, *i.e.* pad layout and certain physical or material properties of the package and base PCB combination (thickness, dielectric permittivity, etc.) can have higher capacitance values than required, making the optimization target impossible to be accomplished. For instance, the equivalent capacitance C_{open} of an open ended microstrip line corresponding to the pad edge as part of the base PCB footprint (*e.g.* Fig. 2b) is just the minimum feasible capacitance of that edge calculated from

$$C_{open} = \frac{\tan\left(\dfrac{2\pi\Delta_{open}}{\lambda}\right)}{2\pi f Z_0} \tag{5}$$

based on the identity between C_{open} reactance and the input impedance of an ideal transmission line of electrical length Δ_{open} (equivalent line length extension due to open end termination) obtained from [5]:

$$\frac{\Delta_{open}}{h} = 0.412 \cdot \frac{\varepsilon_{eff} + 0.3}{\varepsilon_{eff} - 0.258} \cdot \frac{\dfrac{w}{h} + 0.262}{\dfrac{w}{h} + 0.813}, \tag{6}$$

where

f = calculation frequency [Hz];
Z_0 = characteristic impedance calculated for a transmission line of w width;
λ = wavelength [m] corresponding to the f frequency;
h = dielectric height [mm];
w = microstrip line or pad width [mm];

If $w/h \leq 1$, the dielectric effective permittivity ε_{eff} can be calculated from relative permittivity ε_r [5]:

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\left(1 + \frac{12h}{w}\right)^{-0.5} + 0.04\left(1 - \frac{w}{h}\right)^2\right], \tag{7}$$

otherwise ($w/h \geq 1$)

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{12h}{w}\right)^{-0.5}. \tag{8}$$

Minimum capacitance assumption mentioned before is not always true because the effect of other parasitic elements has to be considered as well – namely changes of TL width near pad connections and deviations from recommended material and geometry restriction – as they all have a certain capacitive behavior [6]. A solution for compensating to some extent this drawback will be presented in the following section, meant for some specifically designed surface assembly components and their supporting PCBs.

3. Proposed solutions

Coplanar (or coplanar waveguides – CPW) and microstrip transmission lines are usual solution for signal feeding towards surface assembled components, due to layout compatibility with this technology. The signal guiding strips of both TL types may be considered similar with regular pads from assembly point of view, therefore full layout compliance with characteristic rules related to components connection is required. On the other hand, the components coupled to these lines need specific own pads for all RF input or output ports and complementary ground pads for each RF signal port, as can be seen in Fig. 2b. However, this layout solution has restricted flexibility on dimensions and geometry choice, reflected in the narrower connection bandwidth due to non-optimum parasitic components values.

A better control of the parasitic elements and consequently increased bandwidth become possible in case of integrated design procedure used for both PCB and surface assembled components. Further improvement can be achieved only if the general connection structure is properly modified.

3.1. CPW and microstrip coupling

Presence of closely placed, coplanar signal and ground pads for components' surface mounting assembly is readily fulfilled by CPW, a real advantage over microstrip line which needs a specifically added metallic area (connected to the general ground plane by more metal plated via holes) surrounding the signal pad. Because this layout pattern requires well defined relative location of RF signal line and the associated ground plane(s), the assembly positioning options for the surface placed components are rather limited. In order to assist certain critical applications requiring increased

bandwidth of the component and connection ensemble, a novel architecture is proposed [7]. It can be equally used for CPW and microstrip line transitions, but only microstrip solution is shown in Fig. 5 due to clearer view.

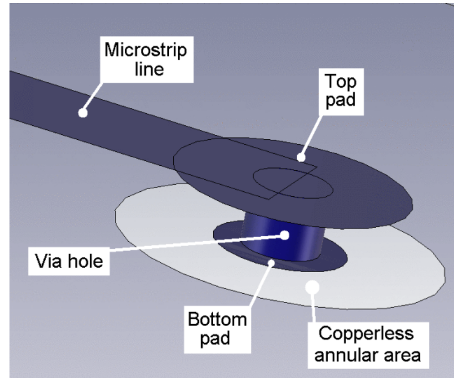

Fig. 5. Novel microstrip transition structure with hidden dielectric substrate.

One may notice a shortcoming of this approach: the connection can be only performed with transitions from stripline (the signal conductor is laid inside dielectric substrate) or other similar structure, because the bottom signal pad is surrounded by general ground plane. Certain real advantages however exist:

- the circular symmetry permits free component rotation around signal via pad axis, a useful feature for multiple positioning assembly;
- there is a larger available range for both via hole and pad diameters because pad dimensions are not more imposed by connection mechanical strength and reliability criteria, but the broadband performance;
- microwave signal radiation is avoided.

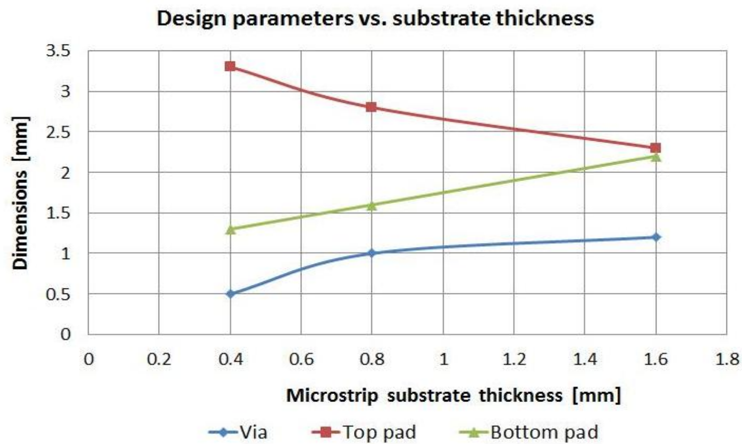

Fig. 6. Main transition parameters vs. substrate thickness.

Figure 6 shows how all pad and via hole diameters change in case of optimum layout design using [4], for different microstrip FR-4 substrate thicknesses; the copperless area was intentionally set to 3.9 mm constant diameter, similar with SMA connector insulator bead. The main limit is set by technological restriction on minimum limit of the hole diameter processing.

A few test structures consisting of short microstrip line segments, each provided with described transition, were manufactured. The experimental results presented in Fig. 7 allow an easy comparison of two cases: (i) single microstrip line with SMA connectors at both ends (continuous lines) and (ii) two cascaded microstrip lines provided with SMA connectors at one end and novel transitions at the other end (dotted lines).

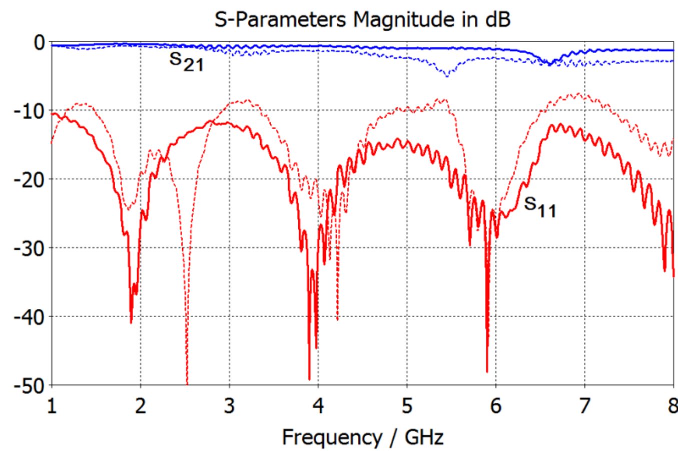

Fig. 7. Measured S-parameters of a microstrip line. Continuous lines: single microstrip results; dotted lines: two cascaded identical circuits provided with novel transition at one end.

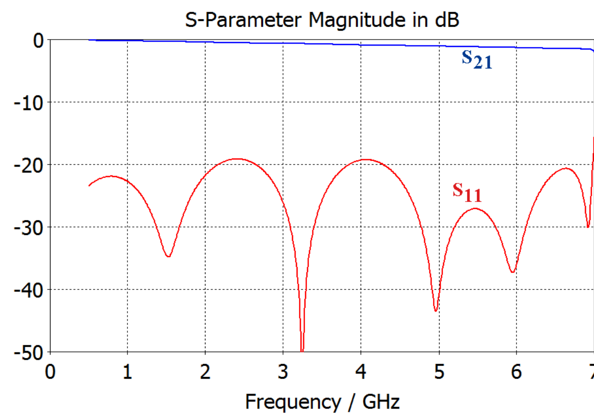

Fig. 8. Simulated S-parameters for the single circuit having measured results in Fig. 7.

Corresponding simulated results for a single microstrip segment (Fig. 8) show a better behavior when compared with measured parameters (continuous lines in Fig. 7). The existing discrepancy can be explained as a result of large tolerance of FR-4 substrate relative permittivity ($\varepsilon_r = 4.3$ was considered for all simulation and optimization processes), therefore characteristic impedance of the microstrip lines is not the expected 50 Ω value, which explains the measured return loss pattern.

3.2. Surface mounting of SIW components

Substrate integrated waveguide (SIW) components can be connected with usual planar transmission lines (microstrip or CPW) by means of specially designed transitions [8]–[9]. Figure 9 shows a specific tapered structure used for microstrip line coupling. Small ground pads can be observed on both sides of the microstrip line ends, normally used in conjunction with CPW probes [10]. There are some drawbacks for this kind of connections:

- they are intended for test purpose only, not for component cascading;
- the existing test probes are very expensive and require coupling to specialized measuring equipment;
- the input/output microstrip lines are quite long in case of broadband matching (CPW transitions are shorter), therefore a wide area around SIW component is lost.

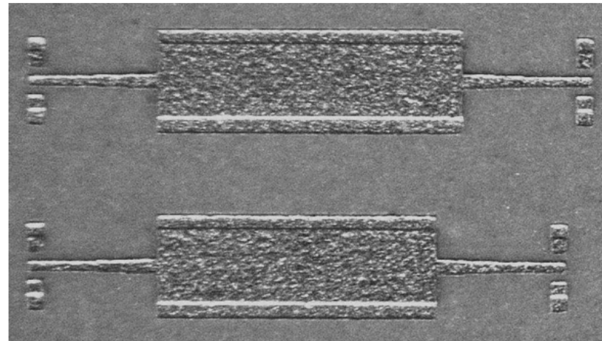

Fig. 9. Example of tapered SIW to microstrip line transitions.
Ground and signal pads are specifically designed for CPW probes [10].

A recent paper presents the first available transition from SIW circuits to small coaxial connectors, also suitable for the building block concept illustrated in Fig. 10 [11]. In fact, the signal pads have a simple configuration, of circular symmetry and themselves compatible with junction assembling between components of similar design, including comparable transitions from CPW and microstrip line already presented in Fig. 5.

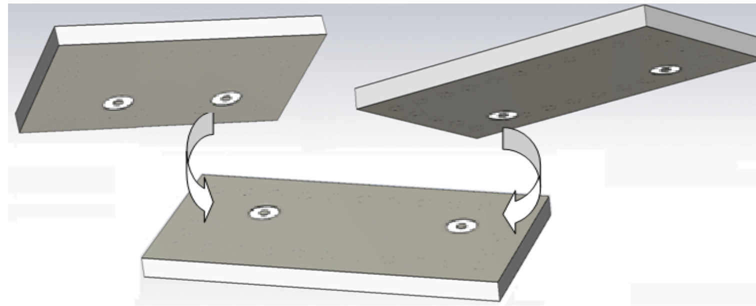

Fig. 10. Building block concept illustration [10].

4. Conclusions

A flexible solution for component packaging based on novel transition compatible with surface mounting assembly technology, intended for connection bandwidth increasing, has been presented. Although it was designed for microstrip and coplanar transmission lines, compatible versions can be also used with minor layout changes for SIW components connection. The transition placement provides a signal transfer interface within main ground plane so that signal radiation is reduced. It has a circular symmetry, therefore the angular component positioning is not more restricted to certain values as it happens with present circuits. A few microstrip models were manufactured by using PCB technology on FR-4 substrate, but the measured results are not yet in very good agreement with circuit simulations. The explanation consists in large error regarding substrate permittivity value.

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