A Clock Generating System for USB 2.0 with a High-PSR Bandgap Reference Generator

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Abstract. A 48-MHz clock generating system for USB 2.0 with an improved bandgap reference generator is proposed to replace an external crystal oscillator. In order to comply with clock frequency and long term jitter specifications under severe supply noise, the power supply of the DCO is regulated by a low drop-out (LDO) regulator. The reference voltage for the LDO is generated by the bandgap reference generator with two bandgap cores to improve supply rejection. The proposed clock generating system implemented in a 130 nm CMOS process shows ± 2.5 ns jitter under ± 400 mV supply noise.

1. Introduction

External crystal oscillators are widely used for the universal serial bus (USB) [1] system to generate a high-precision clock. But, for some applications such as smart card systems, it is difficult to adopt external crystal oscillators because of the small package form factor. Moreover, low power, small area, and low cost are getting more important for mobile systems; hence the clock generator needs to be implemented on chip. The USB 2.0 full-speed specification requires that differential data transitions have 12 MHz $\pm 0.25\%$ frequency and ± 4 ns long term jitter at 14th data edge. In order

to comply with this specification, the clock source should be able to precisely control the clock frequency and suppress the impact of supply noise on the output clock.

Figure 1 presents a simplified block diagram of the 48 MHz clock generating system which consists of a low-dropout regulator (LDO), a bandgap reference generator (BGR), a digitally controlled oscillator (DCO), and a successive approximation register (SAR) digital controller. The BGR generates the reference voltage (V_{REF}) for the LDO and the DCO. The LDO regulates the power of the DCO which is very sensitive to the power supply variation. The SAR digital controller keeps the output frequency the same as the specified frequency, 48 MHz. In order to detect and adjust the DCO output frequency, the SAR controller uses a pulse signal, start of frame (SOF) which is generated every 1 ms by the USB host. The SAR digital controller counts the DCO output clock during a single period of the SOF signal and adjusts the frequency control word (Con[9:0]). The reference voltage, V_{REF} for the LDO should be immune to process, voltage, and temperature (PVT) variations because the variation of V_{REF} has a direct impact on the LDO output voltage and the DCO output frequency.
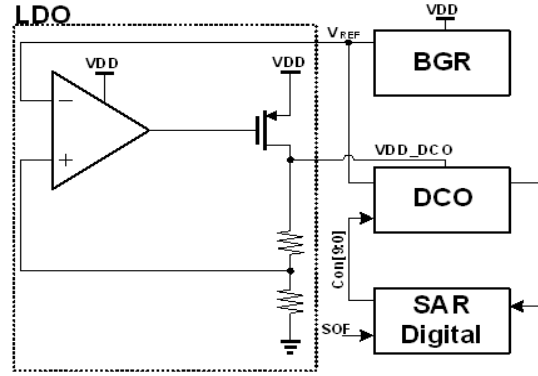

Fig. 1. Simplified block diagram of the 48 MHz clock
generating system for the USB 2.0.

In this paper, we propose a clock generating system immune to supply noise. A bandgap reference generator with enhanced power supply rejection (PSR) is employed to make a stable output clock under noisy supply. This paper is organized as follows. Circuit details and simulation results of the implemented circuits are described in Section 2. The test setup and measurement results such as the long term jitter performance of the clock are presented in Section 3. Finally Section 4 concludes the paper.

2. Circuit implementation

2.1. Bandgap Reference Generation Circuit

BGR is commonly used for ADC, DAC, and many other systems which require a stable reference voltage over PVT variations. To mitigate the impact of the supply noise on output clock, power supply rejection (PSR) of each component inside the

overall clock generation system should be improved. Especially PSR of the BGR is critical because it provides the reference voltage for the LDO. Figure 2 shows a conventional BGR with a start-up circuit [2]. To improve PSR, NMOS and PMOS transistors are cascoded in the BGR core circuit. However, this circuit still has supply dependence due to the channel-length modulation, and the simulated PSR level is not high enough to suppress the power supply noise.
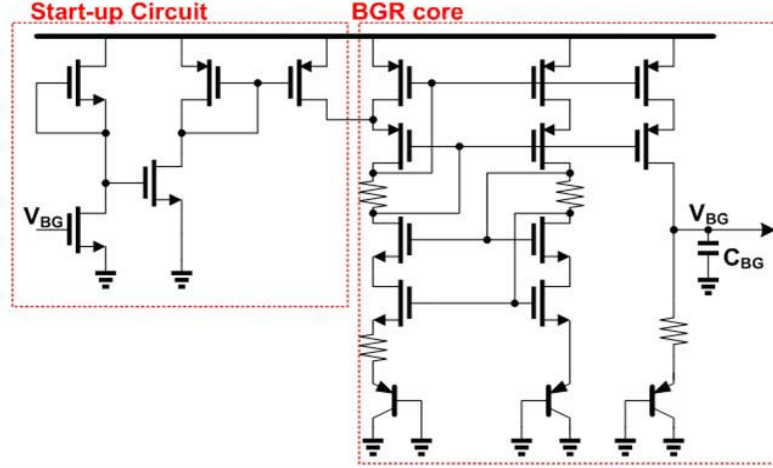

Fig. 2. Conventional bandgap reference generator with start-up circuit.

2.1.1 Supply Regulated Bandgap Reference Generation Circuit

In order to further enhance the supply rejection, the supply voltage of the BGR core is regulated as shown in Fig. 3 [3]. To generate the local supply voltage (V_{DDL}), output voltage of the BGR core (V_{BG}) is utilized as the reference voltage of the local regulator. Power supply noise within the bandwidth of the local regulator is suppressed; therefore the low-frequency PSR can dramatically be improved. However, one of the critical noises on the USB system is the noise induced by USB I/O signals which has relatively high frequency, 12 MHz. To improve PSR at high frequencies, the bandwidth of the local regulator should be extended. But it does not exceed 1 MHz with a reasonable power budget. Another way to solve this problem is using an additional low pass filter with C_{BG} which can filter out the high frequency noise coupling from the power supply. However, this additional C_{BG} makes the output of the BGR rise slowly during start-up process. The internal regulated supply (V_{DDL}) as well as V_{BG} should quickly ramp up to successfully start up the BGR. As the V_{BG} which is the reference voltage for the regulator rises slowly, V_{DDL} also ramps up slowly; the start-up may eventually fail. The start-up problem can be mitigated to some extent as R_{BG} in Fig. 3b is employed and the feedback node (V_{BG_FB}) is separated from the output node (V_{BG}) where C_{BG} is directly attached. In this case, we need a huge R_{BG} because the impedance looking into the BGR from the feedback node (R_{OUT}) is already very high due to the low bias current and the cascoded

structures. At some process corners or extremely low temperature corners, the start-up problem gets worse and the BGR circuit has long start-up time or does not operate at all. Figure 4 shows the effect of C_{BG} on the start-up operation of the conventional supply regulated BGR. In this simulation, R_{BG} is set to zero. It is clearly shown that as C_{BG} is increased, the start-up time gets longer and the output voltage cannot reach the desired level. Because of the start-up problem shown in Fig. 4, a large C_{BG} is not allowed; therefore, there is a limitation in improving high-frequency PSR. A start-up circuit, the supply voltage of which is connected to the global supply (V_{DD}), can be considered to avoid this issue. However, any devices located between the global supply and the BGR core result in significant supply sensitivity and deteriorate the PSR performance.
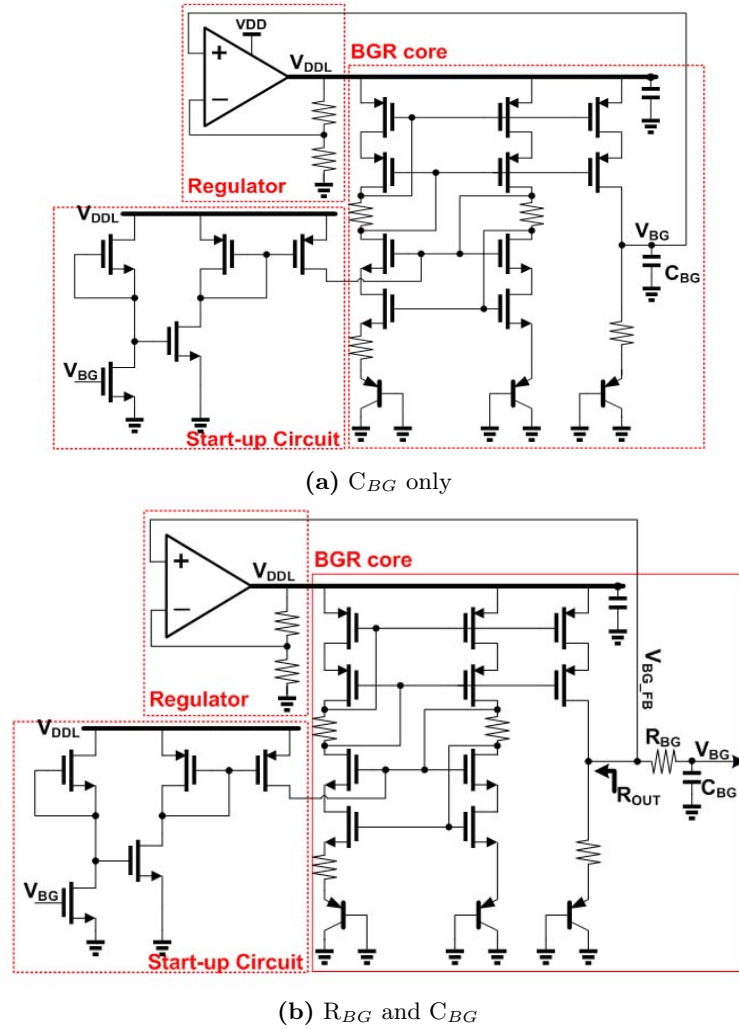

(a) C_{BG} only

(b) R_{BG} and C_{BG}

Fig. 3. Conventional supply regulated bandgap reference generator.

In the following section (Section 2.1.2) we describe two BGR circuits that resolve the start-up issue in the conventional supply regulated BGR and improve PSR in high frequencies.
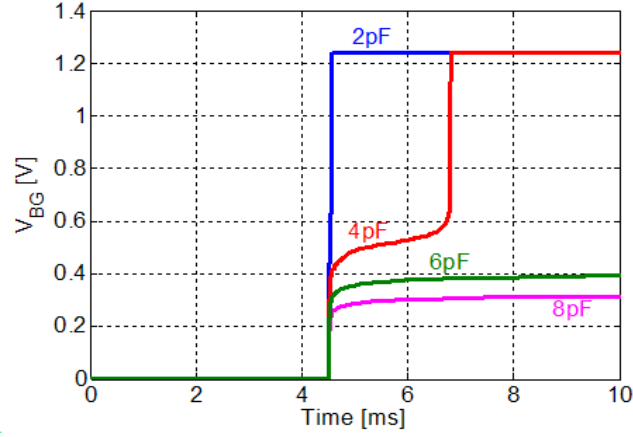

Fig. 4. Simulated start-up behavior of conventional supply regulated bandgap reference generator (C_{BG} is varied from 2 pF to 8 pF).

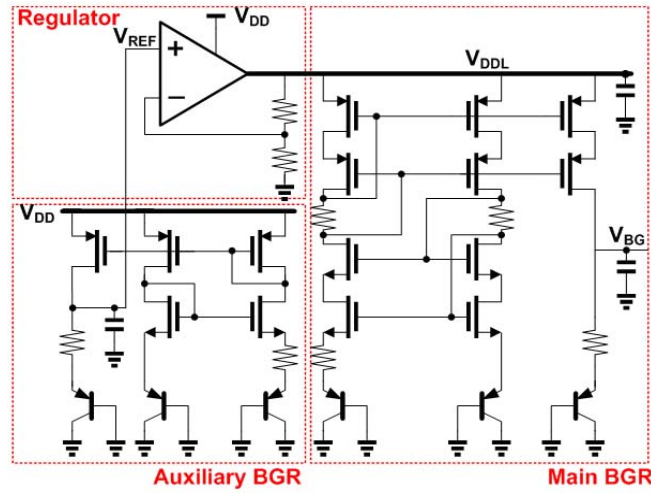*2.1.2 Improved Supply Regulated Bandgap Reference Generation Circuit*

Fig. 5. Supply regulated bandgap reference generation circuit with 2 cascaded cores.

Despite the start-up issue, the supply regulation topology is still attractive in improving low-frequency PSR. To improve high-frequency PSR performance without

the start-up issue while keeping the concept of supply regulation topology, the conventional supply regulation structure is revised as shown in Fig. 5. To exclude the feedback path from the output of the BGR, the auxiliary bandgap core is employed for generating the reference voltage (V_{REF}) of the regulator. When the global supply voltage (V_{DD}) ramps up during power-up sequence, V_{REF} is determined by the output of the auxiliary BGR instead of V_{BG}. The start-up process of the local power supply (V_{DDL}) depends only on the auxiliary BGR which is located out of the feedback path and does not have any start-up problems. Since there is no limit on the choice of C_{BG}, high frequency PSR performance can be improved to the satisfactory level. However, low-frequency PSR performance of the design is relatively worse than conventional supply regulation topology, because the variation of the power supply is directly added to the input of regulator through the auxiliary BGR.
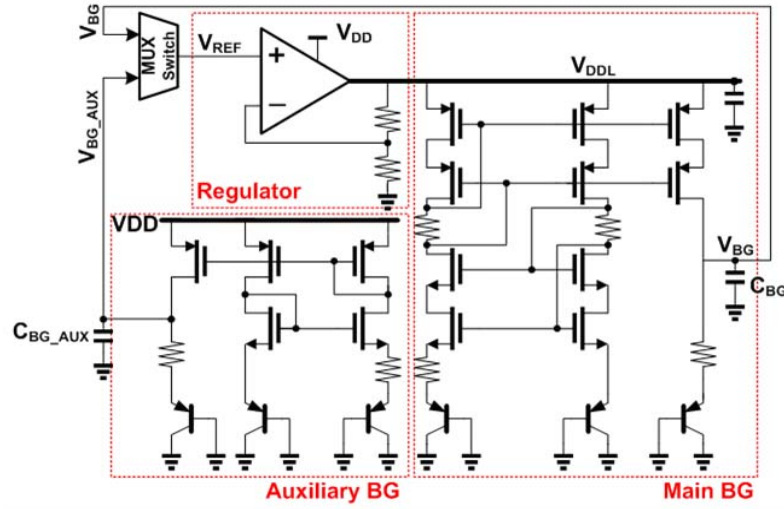

Fig. 6. Supply regulated bandgap reference generation circuit with 2 cascaded cores and multiplexer.
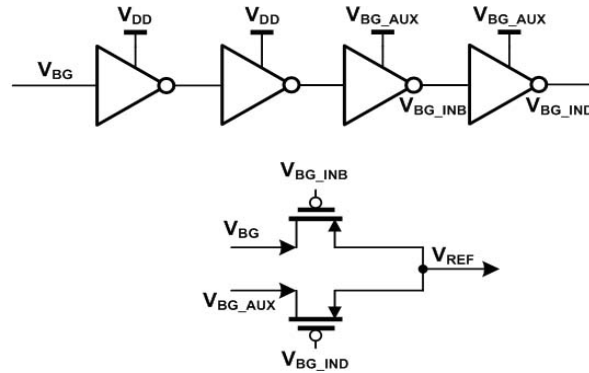

Fig. 7. Schematic of the multiplexer switch.

To achieve further improvement, a multiplexer switch is inserted between the auxiliary BGR and the regulator as depicted in Fig. 6. The input of regulator is initially connected to the output of the auxiliary BGR (V_{BG_AUX}) when global supply (V_{DD}) ramps up during the power-up sequence. Since C_{BG_AUX} is much smaller than C_{BG}, V_{BG_AUX} quickly ramps up. Even though V_{BG} goes up slowly due to the large C_{BG}, there is no start-up issue because there is no feedback from V_{BG} to the regulator until the start-up is completed. After V_{BG} goes up, the reference voltage of the regulator (V_{REF}) is changed to V_{BG} instead of V_{BG_AUX} by the multiplexer switch, and then V_{DDL} is regulated with the feedback of V_{BG} as in the conventional supply regulation topology shown in Fig. 3. Thus, high frequency PSR performance can be improved while keeping the low frequency PSR performance at the same level as that of the conventional supply regulation topology.

Figure 7 shows the detailed schematic of the multiplexer switch in Fig. 6. In Fig. 7, V_{BG_AUX} is from the output of the auxiliary BGR, V_{BG} is from the main BGR, and V_{REF} is the reference voltage of the regulator in Fig. 6. The gates of PMOS transistors in Fig. 7 are controlled by V_{BG_IND} and V_{BG_INB} which are generated from V_{BG}. The first inverter is skewed with the pull-down NMOS stronger than the pull-up PMOS. It detects whether the voltage level of V_{BG} is higher than a certain threshold voltage level ($\sim$0.8 V). Since V_{BG} ramps up very slowly due to the large C_{BG}, relatively large dynamic current flows from the power supply of the inverter to the ground. So, the first and second inverters are powered by V_{DD}, not by V_{BG_AUX}. Otherwise, V_{BG_AUX} can drop considerably, resulting in a start-up problem. According to the level of V_{BG}, V_{REF} is selected either V_{BG_AUX} or V_{BG}.

Figure 8 shows the simulated start-up behavior of the BGR generation circuit in Fig. 6. Before V_{BG} rises, V_{REF} is from V_{BG_AUX}. After the level of V_{BG} ramps up sufficiently, V_{REF} starts to follow V_{BG}. Since V_{BG_AUX} is the output of the simple BGR which is directly powered by global power, V_{BG_AUX} always settles earlier than V_{BG} ramps up. Figure 9 demonstrates that V_{BG} can be reliably generated in all extreme process, voltage, temperature corners by using the switched supply regulation topology in Fig. 6.
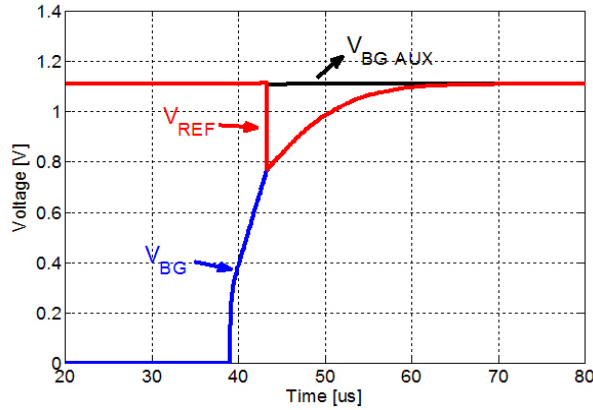

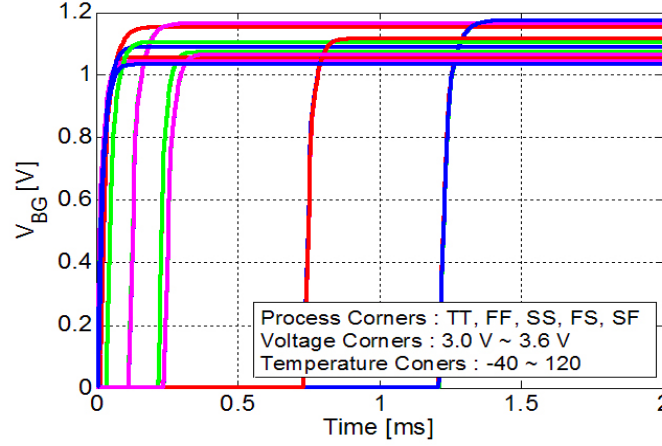**Fig. 8.** Simulated start-up behavior of the multiplexer switch.

Fig. 9. Simulated start-up behavior across the various corners.

Figure 10 shows the simulated PSR of three types of BGR circuits introduced in this paper. BGR1 is the conventional supply regulated BGR circuit in Fig. 3, BGR2 is the supply regulated BGR circuit with 2 cascaded cores in Fig. 5, and BGR3 is the switched supply regulation topology proposed in Fig. 6. BGR1 has relatively high PSR at the low frequency region due to the supply regulation with the feedback from the bandgap output voltage. BGR1 has C_{BG} of only 4 pF which is limited by the start-up problem as shown in Fig. 4 and it leads to poor high frequency PSR performance. On the other hand, BGR2 has much better high frequency PSR performance because BGR2 can have relatively large C_{BG} without any start-up issue. As mentioned above, low frequency PSR performance of BGR2 is degraded by the effect of auxiliary BGR which located out of the feedback loop. Figure 10 also demonstrates that the problem of BGR2 can be resolved by adding multiplexer switch in BGR3. That is, the low-frequency PSR of the BGR3 is comparable to that of BGR1 while the high-frequency PSR is also as good as that of BGR2.
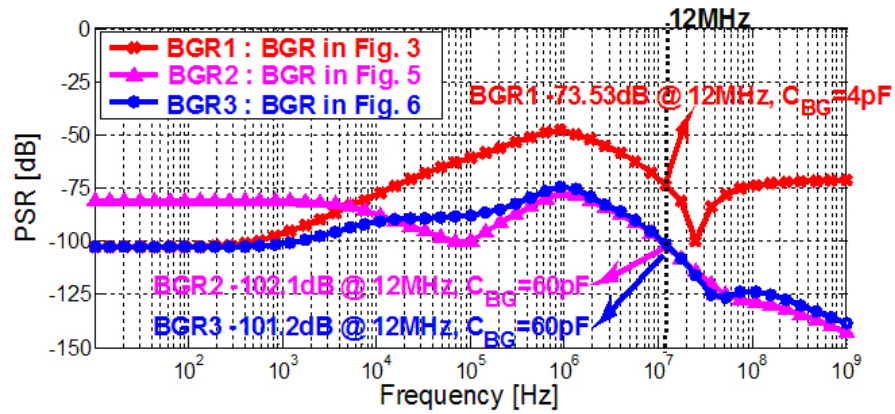

Fig. 10. Simulated PSR of three types of BGR circuits.

2.2. Digitally Controlled Oscillator (DCO)

The DCO in Fig. 11 generates the clock for the system. The frequency of the DCO output clock can be controlled by changing the 10-bit control word (Con$< 9 : 0 >$). The control word is adjusted by SAR digital controller as illustrated in Fig. 1. The DCO consists of a binary controlled current source, a reference current generator and a ring oscillator. The supply of the DCO (V_{DD_DCO}) is regulated by the LDO which employs the output of proposed BGR circuit as the reference. In addition, the reference current is also generated from the BGR output voltage. The frequency of the DCO output clock can cover a range from 38 MHz to 58 MHz by 1024 steps. That is, the frequency resolution is about 19.5 KHz. Figure 12 shows the simulated and measured output frequency of the DCO.
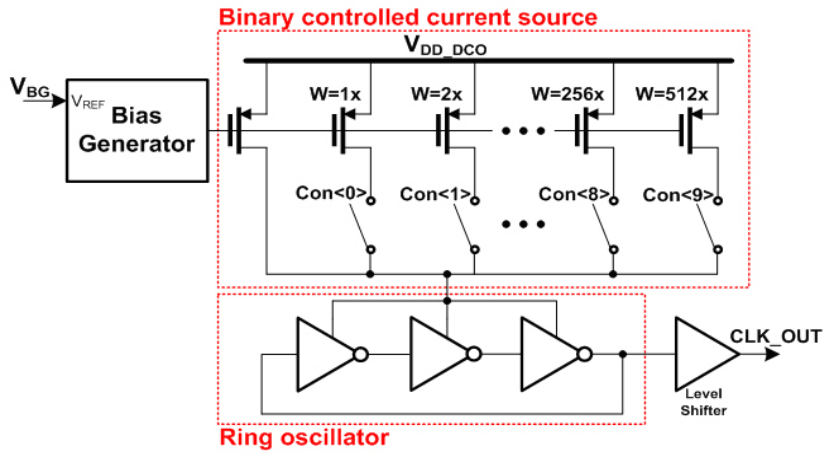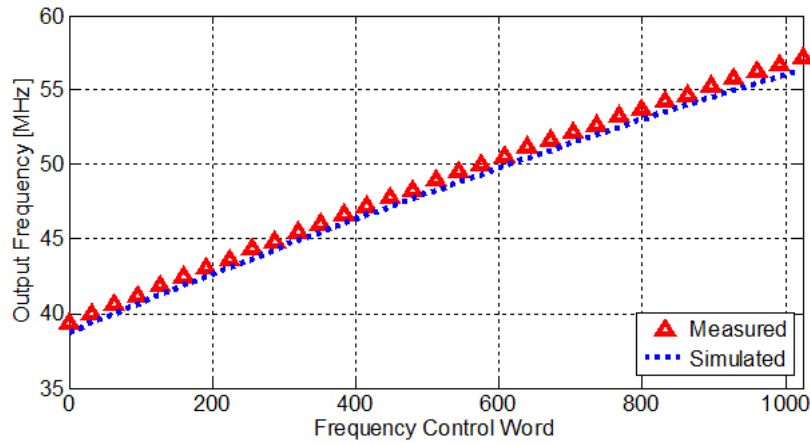

Fig. 11. Digitally controlled oscillator.

Fig. 12. Measured output frequency of the DCO.
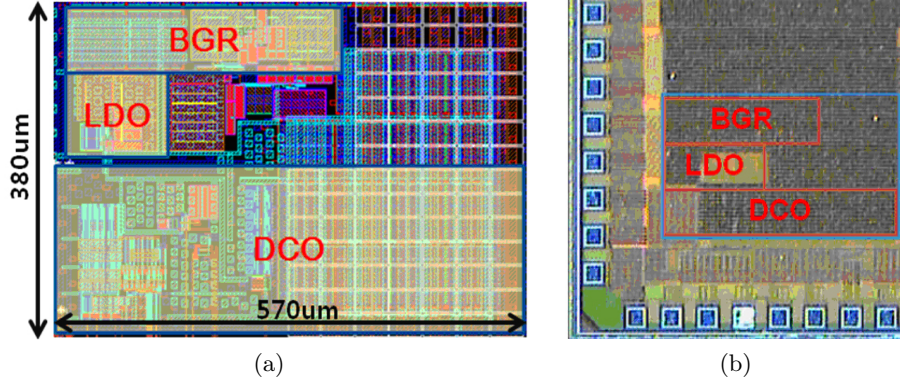
3. Experimental Results

Fig. 13. (a) layout, (b) microphotograph of the clock generating system.

The clock generating system including the supply regulated BGR circuit with 2 cascaded cores is implemented in a 130 nm CMOS process. The layout and the microphotograph are shown in Fig. 13a and Fig. 13b respectively. The chip area is 570 μm × 380 μm and the current consumption of the system is 7.52 mA from a 3.3 V power supply assuming the 48 MHz output frequency. According to the USB 2.0 specification, the quality of the output clock is evaluated with measuring the jitter at every 56th clock. This long term jitter should be bounded within ±4 ns. Figure 14 depicts the measurement setup and evaluation board, where AC noise signal is injected to the V_{SS} to evaluate the immunity to the supply noise. Figure 15 shows the amplitude of the measured power supply noise when the magnitude of the injected noise pulse (V_{noise}) is ±400 mV. Figure 16 shows the long term jitter at 56th clock when 12 MHz noise signals are applied to V_{SS}. The jitter under no additional noise (±30 mV noise still exists due to the measurement circumstance) is ±2.0 ns. When the amplitude of the injected noise pulses are ±200 mV and ±400 mV, the jitter numbers are ±2.1 ns and ±2.5 ns, respectively. It is confirmed that even though the noise is increased, the jitter is not much increased and the system performance still complies with the specification.
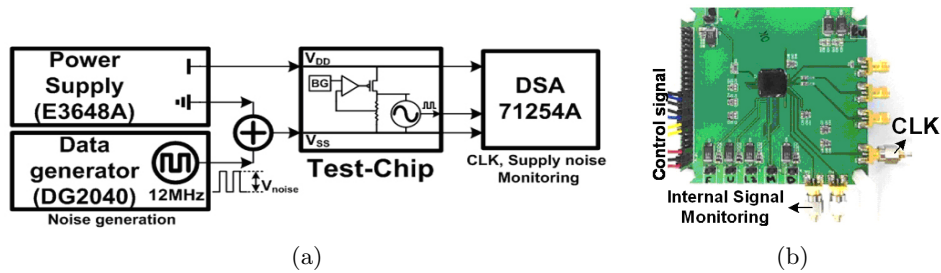

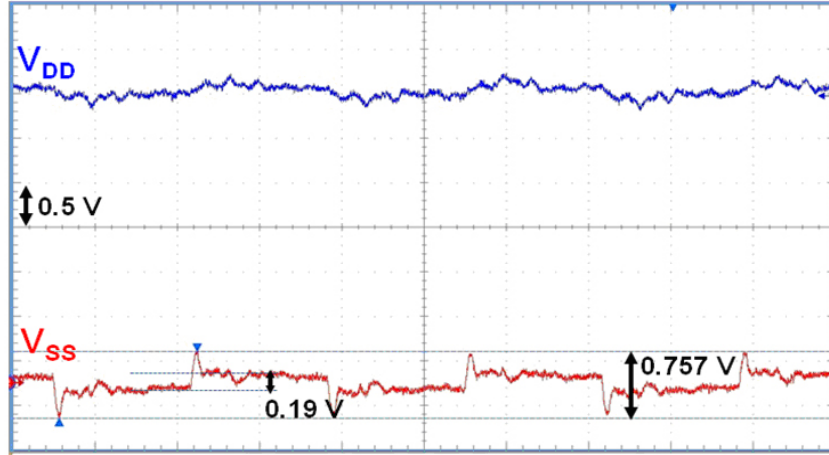**Fig. 14.** (a) Measurement setup, (b) evaluation board with COB.

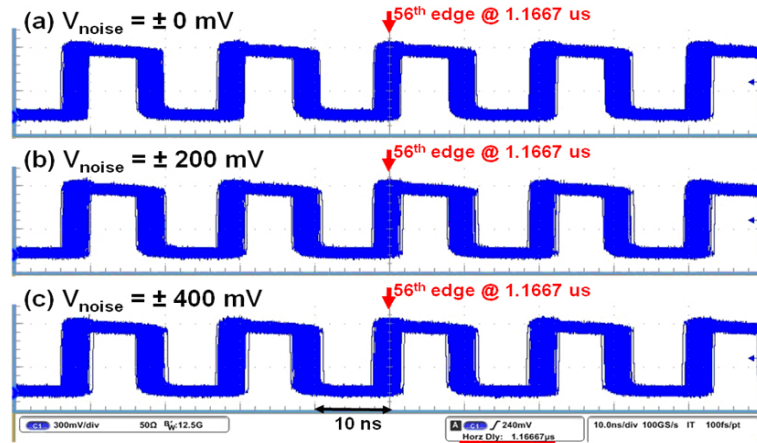**Fig. 15.** Measured power supply under V_{SS} noise (V_{noise} = ±400 mV).

Fig. 16. Measured jitter under V_{SS} noise.

4. Conclusion

In this paper, a clock generating system for USB2.0 with an enhanced bandgap reference circuit is proposed. To improve the PSR of the BGR circuit, 2 cascaded bandgap cores are used in the implemented test chip Experimental results confirm that the long term jitter of the proposed circuit is immune to the VSS noise. So the proposed clock generating system can be a key solution for design of USB system without external crystal oscillators.

References

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