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# Integrated Dual-chain Dickson Charge Pump optimized for Resistive Loads

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**Abstract.** The proposed circuit is a dual-chain Dickson type charge pump making use of both active and passive charge transfer switches in order to achieve a compromise between power efficiency, circuit complexity and device reliability. The charge pump is capable of sourcing up to 500 μA at 10 V output voltage for supplying the error amplifiers of two NMOS Low Drop Out (LDO) linear regulators as part of a high integration automotive IC.

**Key words:** Dickson charge pump; NMOS LDO; RC oscillator.

## 1. Introduction

One clear trend in automotive electronics is pursuing a higher level of integration as a method of managing the rise in complexity at the system level and increasing the reliability and energy efficiency of automobiles. In high level integration ICs instead of the conventional PMOS LDO topology an NMOS power transistor can be used as a pass device on considerations of smaller silicon area and better dynamic performance. In order to drive the NMOS pass device in the deep triode region during low drop-out (LDO) operation a charge pump is needed for supplying the driving stage of the regulator's error amplifier. In order for the regulator to achieve the desired dynamic performance (in terms of load and line jump response) the charge pump needs to have a high output current capability and a fast ramp-up time.

One specific example for these requirements is supplying a strongly non-linear load like a microcontroller or a CPU core which can produce a load jump starting from a base current in the microampere range to the maximum load that the regulator can provide. The current capability necessary for the error amplifier in order to quickly charge up the gate of an NMOS pass device of a fast LDO must be delivered by using

the smallest possible silicon footprint while also choosing the clock frequency so as to avoid excessive EMI.

Basically the NMOS LDO approach only makes sense if the sum of the silicon area required by the charge pump and the area required by the NMOS pass device is smaller than the equivalent area of a PMOS pass device. While not always a good solution for a single LDO, the described approach becomes especially attractive for power management units (PMUs) or system basis chips (SBCs), namely monolithic circuits that integrate multiple LDOs sometimes alongside synchronous Buck or Boost DC-DC converters.

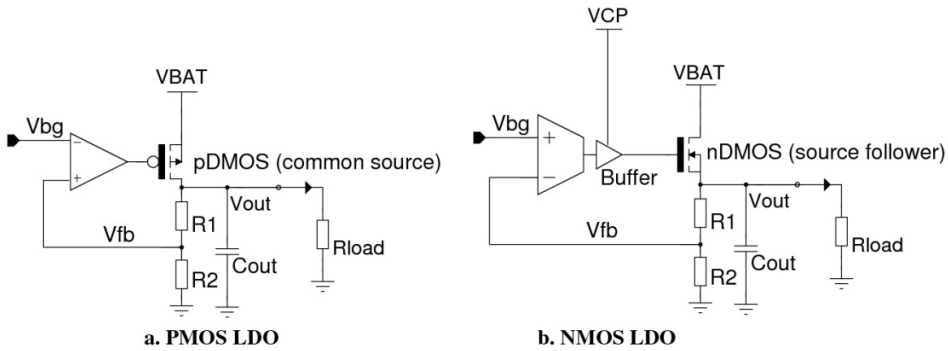


**Fig. 1.** Comparison between LDO topologies.

Many of the monolithic charge pump circuit implementations are based on the Dickson topology [1] using some form of passive (mainly PN junction or CMOS diodes) or active charge transfer switches separating the pumping capacitors.

The main advantage of passive charge transfer switches is their inherent simplicity given by the fact that they don't require dedicated control signals in order to initiate/stop the charge transfer process. The self-on/self-off behavior can simplify the structure of charge pumps. However, when the charge pump circuit has increased output current requirements or it is integrated in a low voltage system, the basic Dickson structure (using only some form of diodes) suffers from limitations resulting from the incomplete charge transfer of the passive switches. This drawback is even more apparent on the last cascaded stages where the high source to bulk potential difference of the diode connected transistors increases the threshold voltage leading to increasingly high charge transfer losses. Active charge transfer switch implementations solve the gain degradation problem with the price of increasing the complexity of the circuit by using multiple non-overlapping clock signals in order to precisely control the on/off behavior of the switches and voltage boosted topologies in order to decrease the equivalent impedance of the switches and improve the charge transfer efficiency.

The proposed charge pump core uses a mixed active [5] and passive charge transfer switch implementation. The passive charge transfer switches are implemented using diode connected NMOS transistors. Bulk/body bias is used for these transistors during the charge transfer phase in order to lower the threshold voltage and improve

charge transfer efficiency. This topology was chosen for the realization of the charge pump core in order to reach a compromise between efficiency and complexity.

## 2. Concept and design

### A. A system perspective

The proposed charge pump circuit block diagram is presented in Fig.3. The Dickson-type CP core generating the high voltage output *VCP* is driven by a simple RC oscillator. A simpler approach would have been to use appropriately sized inverters in a current-starved ring oscillator structure as a means of both generating the clock signal and driving the pumping capacitors as exemplified in Fig. 2. With the aid of trimming circuitry for the bias current and supplied from a regulated voltage rail the current-starved ring oscillator/driver topology can fulfill the requirements of a surprisingly large number of charge pump circuits.

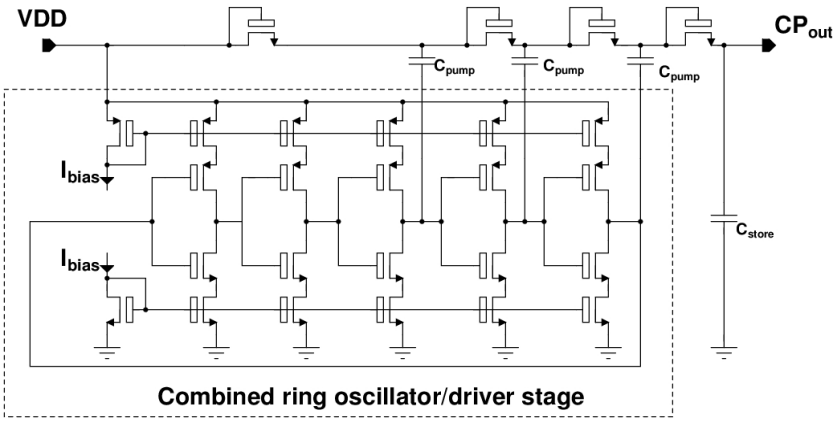


**Fig. 2.** Integrated charge pump using combined ring oscillator/driver stage approach.

However, as already stated this approach was abandoned in favor of an RC oscillator and dedicated drivers for the pumping signals. One advantage of using an RC oscillator is the fact that it can effectively eliminate part of the charge pump current capability spread with process variations. Usually, during the implementation of an RC oscillator a low voltage capacitor is used, given the fact that the clock generation circuitry and the charge pump core can be in different voltage domains. If the frequency is chosen to be high enough, the same type of capacitor as the main pumping capacitors inside the charge pump can be used without an area penalty even if a higher than necessary voltage class capacitor is used in the oscillator.

Although it seems counter-intuitive to spend the additional area for a higher voltage class capacitor, in fact, matching the capacitor type inside the charge pump core and to the capacitor type used in the oscillator has the effect of partially canceling the variation of the charge pump current capability with the pumping capacitor

value. To a first order approximation an increase in the specific capacitance would lead to a lower clock frequency but also to higher valued pumping capacitors, keeping the current capability constant. A decrease in specific capacitance would lead to lower valued pumping capacitors but also to a higher clock frequency also keeping the current capability constant.

In order to reduce the cross currents through the charge pump drivers the classical inverter structure was replaced by a simple "brake-before-make" circuit topology. This was preferred with respect to a current starved driver approach owing to its simplicity, reduced area requirements and smaller influence on the non-overlapping nature of the control signals.

Given the fact that the charge pump is automatically turned on only when one or both of the LDOs are operating it will always be loaded by the error amplifiers so there is no need for some form of active output voltage regulation.

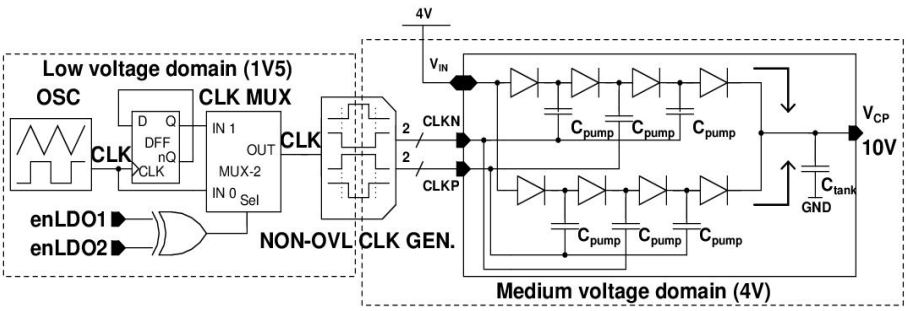


**Fig. 3.** The proposed CP topology.

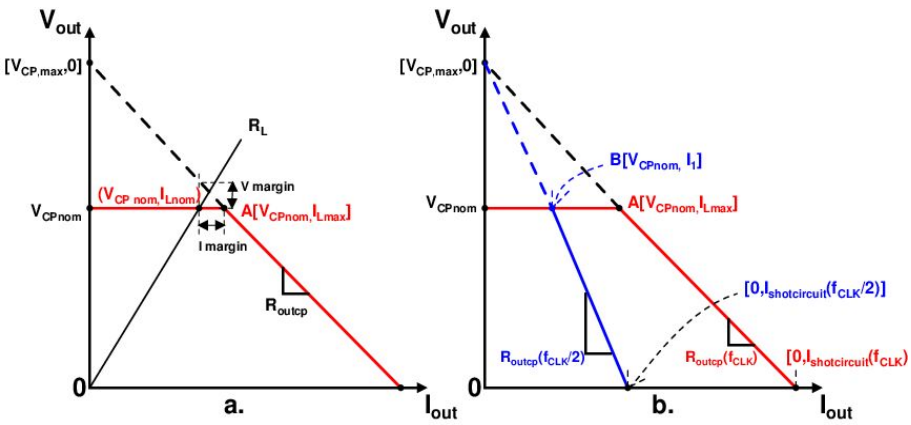


**Fig. 4.** Static transfer characteristics.

When one of the regulators is turned off, the frequency coming from the oscillator is simply divided by two also halving the current capability as a result. A series combination of Zenner and bipolar junction diodes exhibiting minimal temperature

dependence is used as a clamping circuit to sink the excess current. This clamping circuit activates only when there is a mismatch between the load (LDO error amplifiers) and the current capability of the charge pump (higher current capability of the CP core in some technological corners) or at very low LDO loads (when also the error amplifiers have lower bias current requirements).

A standard automotive BCD technology was used, thatprovides several CMOS voltage classes: low voltage (1.5 V) analog and logic transistors, several types of medium voltage analog transistors and high voltage (60 V) DMOS power transistors as well as bipolar diodes and transistors.

The static transfer characteristic of a CP designed for resistive loads is presented in Fig. 4a.

The CP is sized to provide the maximum DC current $I_{L,max}$ corresponding to point $A(V_{CPnom}, I_{L,max})$ on the transfer curve. $V_{CP,max}$ is the maximum unclamped voltage the CP core is capable of delivering if the load current is zero. If the CP is delivering the maximum load current $I_{L,max}$ then the voltage clamp sinks no current because the output voltage is already at the desired level $V_{CPnom}$. Otherwise, if only one of the LDOs is working, in order to avoid sinking current through the Zenner clamp the frequency of the CP core is halved increasing the output impedance of the CP core. This operating condition is described by point B in Fig. 4b.

The clock signal generated the on-chip RC oscillator (in the 1.5 V voltage domain) is divided by two and fed along with the non-divided signal into a simple multiplexer which drives the actual charge pump core. The clock frequency selection is made by the multiplexer depending on how many LDOs are active.

### B. The charge pump core implementation

The implemented charge pump core pictured in Fig. 5 consists of two Dickson pumping chains working in anti-phase. A very similar approach was used by our design team in [4]. In order to ensure a lower ripple on the output voltage, charge is transferred to the $C_{tank}$ reservoir capacitor every semi-period [6] (making the effective pumping frequency $2f_{CLK}$).

For the proposed Dickson-type CP architecture delivering the $I_L$ load current, implemented with N pumping stages and M pumping chains, using identical $C_p$ pumping capacitors, having $C_S$ total stray capacitance in each pumping stage, supplied by $V_{CLK}$ and driven by a $f_{CLK}$ frequency clock we can write:

$$V_{CP} = V_{CLK} + N \cdot \left[ \frac{C_P}{C_P + C_S} \cdot V_{CLK} \right] + (N-1) \cdot V_D - \frac{N \cdot I_L}{M \cdot (C_P + C_S) \cdot f_{CLK}} \quad (1)$$

Only the first (N-type) and the last (P-type) switch in each pumping chain are the active type and have no voltage drop during charge transfer, while the rest of the diode-type switches with the bulk connected to the drain, have $V_D \approx$500 mV drop. For the implemented CP core we have N=3, M=2 , $V_{CLK}$=VDD4V $\approx$ 4 V and $f_{CLK} \approx$16 MHz.

The single phase low voltage (1.5 V) domain *Clk* clock input driven by the clock mux is fed to a non-overlapping clock generator that delivers four non-overlapping

phases each having a 4 V amplitude to the CP core. For this purpose, a simple 2 phase non-overlapping clock generator realized in the low voltage domain produces two clock phases and their complements (so effectively 4 phases) that are then level shifted to the medium voltage domain (4 V) to drive the CP core. Several non-overlapping time intervals can be chosen by coupling or decoupling part of the C1a and C1b capacitors (in Fig. 6) inside the clock generator. The possibility to tune the non-overlapping time intervals was added in order to ensure that the voltage signals at the output of the pump drivers still maintained non-overlapping behavior when loaded by the pumping capacitors.In other words it's not enough to ensure non-overlapping control signals at the inputs of the pumping drivers. We must also ensure that the output voltage wave forms of the pump drivers having less steep fronts (because of the loading by the pumping capacitors)still maintain the non-overlapping relationship. This is important because the signals in the pumping nodes of one pumping chain act as boosted control signals for the complementary switches in the other pumping chain.

In order to ensure that charge transfer via the active switches is unidirectional, non-overlapping phase relationship exists between *Clk_NSW* and *nClk_NSW* signals driving the N switches and between *Clk_PSW* and *nClk_PSW* driving the P switches. The chosen topology using both passive and active switches is a good compromise between charge transfer efficiency and system complexity, as an implementation using only active switches would require additional non-overlapping phases and dedicated drivers for each of the pumping capacitors.

The $N_{1A}$ and $N_{1B}$ switches are implemented using medium voltage NMOS devices actively switched in the triode region during charge transfer. The structure is symmetric, the boosted gate signal for one active switch being provided by the previously charged complementary node on the other pumping chain. While charging $C_{1A}$ the control signal for $N_{1A}$ is provided by Node1B and vice versa.

A more detailed explanation of the above statement is given as follows. Considering (like in Fig. 7a) that *nCLK_NSW*is logical zero, the inferior plate of $C_{1A}$ driven by the non-inverting pump driver DRV is at ground level. After a short time (given by the non-overlap interval $t_{novl}$ between *CLK_NSW* and *nCLK_NSW*) the gate of $N_{1A}$ (which is connected to upper plate of capacitor $C_{1B}$ on the complementary pumping chain) is driven to a potential equal to the supply rail of the pumping drivers ($VDD4V$) plus the voltage stored on the previously charged C1B, so effectively to 2 $\times VDD4V$. $N_{1A}$ is thus driven in the deep triode region allowing $C_{1A}$ to charge to *VDD4V*. After the charging phase ($T_{on,N}$) passes, *CLK_NSW* and consequently the control signal for $N_{1A}$ goes to logical zero and closes the $N_{1A}$ switch always well before *nCLK_NSW* drives the lower plate of the now charged $C_{1A}$ to *VDD4V* initiating the charge transfer to $C_{2A}$. The potential in Node1B which is controlling switch $N_{1A}$ is also decreasing during the charging phase of $C_{1A}$ because during this same time $C_{1B}$ is transferring charge to $C_{2B}$ through the open $ND_{1B}$. However this does not have an impact on the efficiency of the charge transfer because $C_{1A}$ is completely charged before the discharge of $C_{1B}$ and the transition of $N_{1A}$ into the saturation region. We can thus safely assume that in steady-state operation the active (N and P) switches are always driven in the deep triode region during the charge transfer phases.

The P-type switches in each pumping chain are implemented using medium voltage

PMOS devices. In order to safeguard against the increased latch-up risk of the PMOS, an active bulk switching mechanism [2] was implemented with the additional $PB_{1A}$ and $PB_{1B}$ transistors by always keeping the bulk of all of the PMOS devices at the highest potential in the circuit and storing this potential on a small capacitor ($C_B$) between refresh phases.

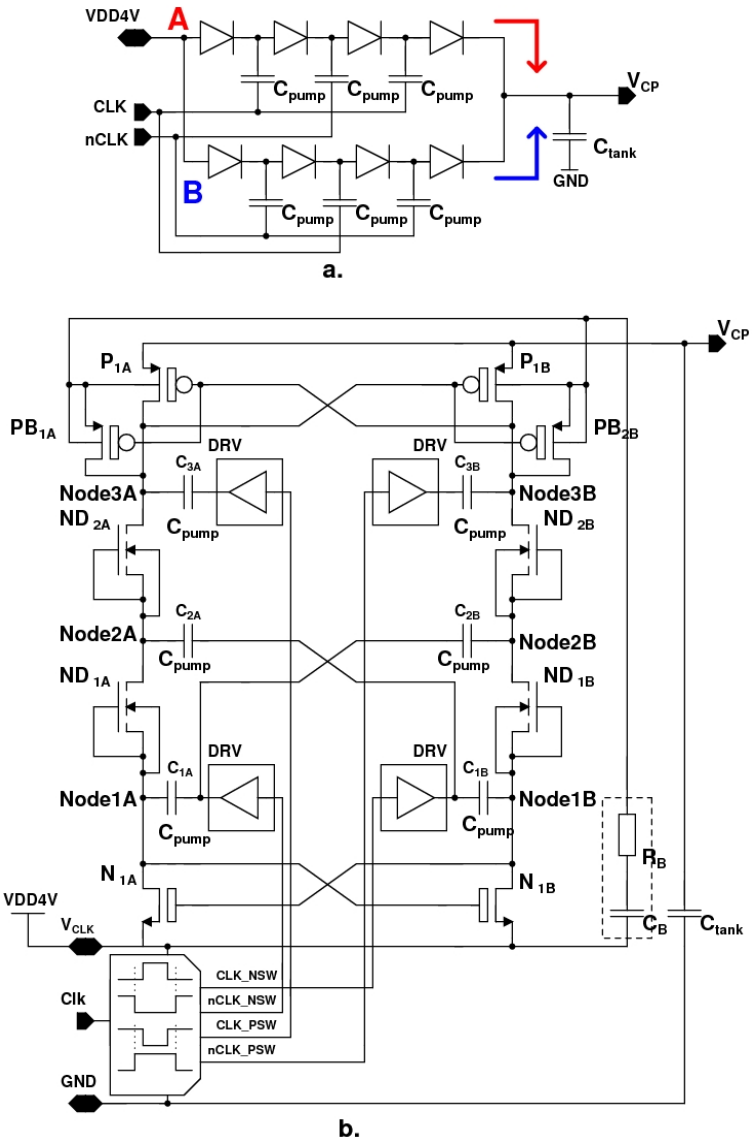


**Fig. 5.** a) Simplified architecture of a Dual-chain Dickson charge pump; b) The implemented charge pump core.

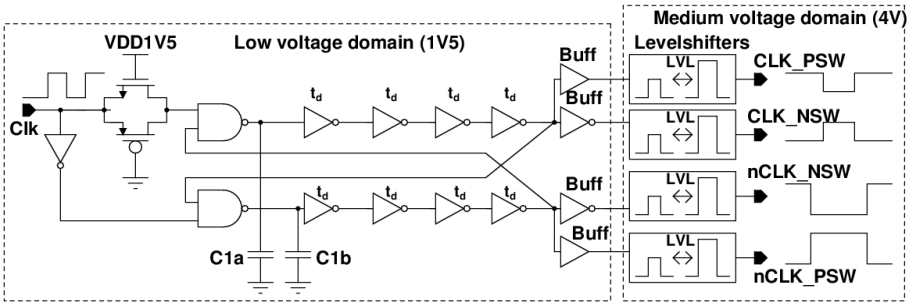


**Fig. 6.** Non-overlapping clock generator.

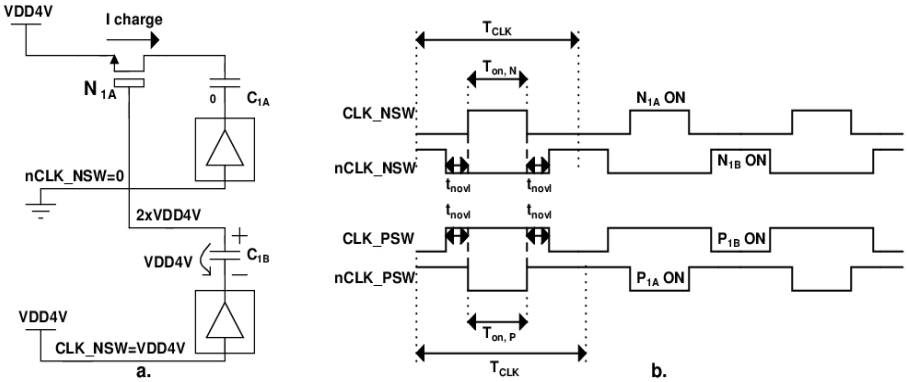


**Fig. 7.** a) Equivalent schematic for charge transfer through $N_{1A}$;
b) CP core clock signal diagram.

In order to better understand the bulk switching mechanism we can analyze the charge transfer process from capacitor $C_{3A}$ to the tank capacitor $C_{tank}$ at the CP output. Considering $C_{3A}$ charged in the previous phase and the *CLK_PSW* signal driven high, the potential in Node3A is equal to the voltage stored on $C_{3A}$ plus $VDD_4V$, and is essentially the highest potential in the CP core (higher than$V_{CP}$). Therefore when $P_{1A}$ is turned on to initiate the pumping phase for $C_{3A}$, the bulk of $P_{1A}$ should ideally be connected to Node3A. However, if we consider the charging phase of $C_{3A}$, the potential in Node3A is significantly lower than $V_{CP}$, making Node3A a poor choice for connecting the bulk of $P_{1A}$. The dynamic bulk switching mechanism is implemented by activating transistor $PB_{1A}$ for connecting the bulk of $P_{1A}$ (and also $P_{1B}$ and $PB_{1B}$) to Node3A but only during the pumping (charge transfer) phase when Node3A has a higher voltage than $V_{CP}$. During the charging phase of $C_{3A}$, when $P_{1A}$ and $PB_{1A}$ are off, the symmetric structure of the CP core ensures that $C_{3B}$ is in the pumping phase with Node3B at the highest potential in the CP core and $P_{1B}$ and $PB_{2B}$both turned on. During this phase the bulk terminals of $P_{1A}$ and $PB_{1A}$ both of them in the off state are connected to Node3B by $PB_{2B}$. As already mentioned, between refresh phases, during the very short intervals when due to non-overlapping

both $PB_{1A}$ and $PB_{1B}$ are turned off, the bulk biasing potential is stored on the $C_B$ capacitor. The bulk switching mechanism is a simple and reliable solution to avoid activating the additional parasitic vertical NPN or PNP structures that exist for PMOS devices and can trigger a latch-up event.

Drain-bulk overstress also prevents the use of active N and P type switches in the other pumping stages and determines $(V_{CLK,max} \approx 4\ V) < |V_{DB,max}|/2$.

The $ND_{1A}$, $ND_{1B}$ passive charge transfer switches are NMOS diodes implemented using another type of medium voltage transistor with access to the bulk terminal. In order to forward bias the bulk source junction and lower the threshold voltage during the charge transfer phase, the bulk connection of the diodes is tied to the drain terminal. In order to verify that the majority of the charge transfer occurs through the transistor channel and not through the bulk to source diodes, test structures of the used NMOS diode configuration have been built and the reverse recovery time and forward drop during charge transfer were measured.

If the bulk to source diodes which are essentially bipolar diodes are responsible for the charge transfer between the pumping nodes, a major concern especially at higher operating frequencies is the reverse recovery time($t_{rr}$). When a bipolar diode is forward biased and carrying forward current there is charge stored in PN junction's diffusion capacitance. The amount of charge stored and implicitly the reverse recovery time and reverse recovery current is strongly dependent on the forward current the diode was conducting before being reverse biased (switched off). The reverse recovery time can be divided into two distinct phases: the storage time and the transition interval as described in Fig. 8. Storage Time ($t_s$) is the required period of time for the minority carriers to return to their majority-carrier state on the other side of the PN junction. Transition interval ($t_t$) is the second time interval when the storage phase has passed and the current is reduced in level to that associated with the non-conduction state.

By contrast, in the strong inversion operating region where the MOS diodes are used, the charge transfer through a MOS transistor is unipolar (only one type of charge carriers) and dominated by the drift component. This means that only minimal reverse recovery behavior and most importantly no correlation between forward current and reverse recovery time should be observed if the majority of the current flowing between the CP nodes is transferred through the channel of the transistor.

As expected, the reverse recovery time was found to be very small and most importantly independent on the value of the forward current flowing through the NMOS diode before the switch-off event. This eliminates the possibility of a bipolar conduction mechanism through the bulk-source diode, proves that the charge is transferred through the NMOS channel and validates the proposed bulk biasing technique. Voltage drop measurements also confirm this hypothesis.

The concept for the pumping capacitor drivers is presented in Fig. 9. A good method of improving the power efficiency of the charge pump core is to reduce the cross current of the pumping capacitor drivers.The "break-before-make" topology used provides a fast discharge path for the gate of the output transistor that needs to be switched-off as fast as possible to avoid cross current while also providing a slow charging path to the gate of the transistor that needs to be switched on during that

respective clock phase. The delay mechanism needed for the slow charging path is realized by using the transistors Nx and Px as voltage controlled resistors through which the large gate capacitance of the respective output transistor (Pdrv or Ndrv) can be charged.

The fast discharge of the complementary output transistor can be done directly by the input inverter (Pin and Nin) having a larger (W/L) ratio than Nx and Px. Consider the low (0 V) to high (4V) transition on the input pin *inDRV*. This will turn on the Nin transistor and the Nx transistor and switch off the Pin and Px transistors. Transistor Ndrv will be quickly switched off by Nin turning on, but the gate of Pdrv is forced to charge through the equivalent Rds(on) of Nx. By appropriately dimensioning Nx, Pdrv will switch on only after Ndrv is fully off.

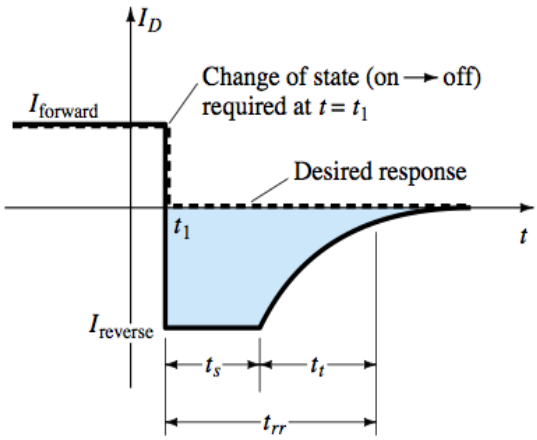


**Fig. 8.** Reverse recovery time. Charge stored in the diffusion capacitance.

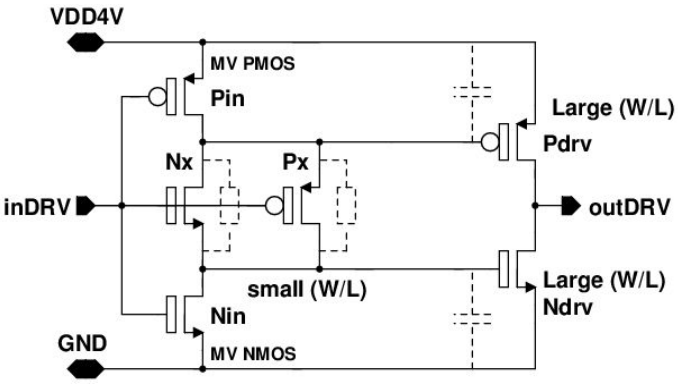


**Fig. 9.** Pumping (charge transfer) capacitor driver.

### C. RC oscillator implementation

The topology for the implemented oscillator was first described in [3] although at a lower frequency. The oscillator was implemented using low voltage (1.5 V) CMOS transistors.

The main advantages of this topology are a rigorously 50% duty cycle owing to the symmetry of the circuit and that in considering a first order approximation the oscillation frequency is set only by the time constant of the integrated resistor and capacitor.Only the resistor spread over process will have an impact on the performance of the system, because as already mentioned, frequency variations caused by the capacitor spread are compensated by using the same type of capacitor in both the oscillator and the charge pump core. The operation is the following. First of all accurate matching needs to exist between the P0, P1 and P4 PMOS transistors and also between the M0, M1 and M4 NMOS transistors. A bias current is generated by subtracting fromthe supply voltage the gate to source voltages of P0 and M0 and dividing the value over R.

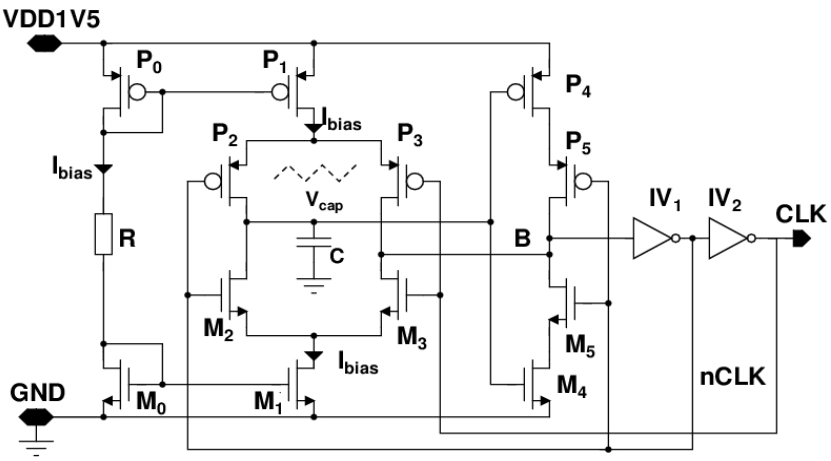


**Fig. 10.** RC oscillator schematic.

Presuming that the output is low, M2, P3, M4 and M5 are open and the previously charged capacitor C discharges linearly, at constant current $I_{bias}$ through M2 and M1. The same discharge current is mirrored by P1, passes through P3 and M5 and is sinked by M4 whose gate is controlled by the falling capacitor voltage. When $VGS_{M4}(I_{bias})$ is equal or slightly below $VGS_{M1}(I_{bias})$ the voltage on point B will rise as M4 cannot sink all of the current injected by P1 thus driving P1 into the triode region. The voltage on net B shaped and buffered by IV1 and IV2 triggers a positive feedback loop that switches the output. Symmetry ensures the same functionality for the charging path. P4 and P5 will conduct the same IBias current as P1 and P2 that are charging C. This is valid until the potential on C determines $VSG_{P4}(I_{bias})$= $VSG_{P1}(I_{bias})$ at which point net B goes to low and the output switches).

An essential point is that if operating at a higher frequency, the delay introduced by charging and discharging the capacitance at node B becomes of the same order of magnitude as the oscillation period, introducing a significant error (as much as 5 %) if $I_{bias}$ is not high enough. The value of R must be chosen so that $I_{bias}$ can charge the capacitance at node B in a much lower time than the desired clock period.

$$I_{bias} = \frac{VDD1V5 - VSG_{P0}(I_{bias}) - VGS_{M0}(I_{bias})}{R} \tag{2}$$

$$\Delta V_{cap} = VDD1V5 - VSG_{P0}(I_{bias}) - VGS_{M0}(I_{bias}) \tag{3}$$

$$T_{CLK} = \frac{2\Delta V_{cap} \cdot C}{I_{bias}} = 2RC \tag{4}$$

The oscillation frequency has a low dependency of the supply voltage variation ($\Delta f/f\Delta V < 0.8\%V^{-1}$ from 1.35 V to 1.65 V) and a low temperature dependency (less than 2% in the whole automotive temperature range from −40°C to 150°C). In both cases the dependencies are generated by the variation of the total capacitance in node B with temperature and bias conditions (body effect of P5 and M5). Several iterations of parasitic back-annotated simulation were necessary to determine the optimum value for C.

## 3. Simulation and measurement results

### A. Simulation results

Figure 11 shows a photomicrograph of the fabricated charge pump test chip. For evaluation purposes, the charge pump as well as the NMOS LDO regulators that the CP supplies and the necessary interface/control logic were integrated on a test chip.

Figure 12 shows the simulated voltage waveforms of the charge pump during ramp-up as well as during the application of a 0 to 600 μA load jump. The simulations depicted in Fig. 12 are done in the nominal technological corner. Corner simulations were also performed in order to evaluate the performance of the circuit with the variation of technological parameters. In order to obtain the maximum amount of coverage with the minimum amount of simulations, the critical test cases were defined as a combination of process variations, temperature and supply voltage values (for both the oscillator and the CP core).

For each of the 12 technological corners considered, the simulations were performed at −40°C and 150°C, with the oscillator supply voltage at 1.35 V and 1.65 V, and the CP core supply at 3.8 V (the worst case for the CP core supply). The simulation results of the 48 resulting test cases are presented in Fig. 13. In order to reduce simulation time, the load was applied by a simple current mirror driven by an ideal current source instead of the actual circuitry that the CP is supplying. An interesting effect that we can observe from Fig. 13 is the separation of the CP output voltage graph family into two sub families separated by a gap. The two sub-families were found to

correspond to the two temperatures at which the simulations were performed. While the voltage clamp at the output of the CP is dimensioned for minimal temperature dependence, an optimal thermal compensation is not achieved if the process deviates significantly from the nominal. However, even in these conditions, for a given technological corner, the difference in output voltage between −40°C and 150°C is not larger than approximately 0.5 V, and more importantly the minimum output voltage while sourcing 500 μA is approximately 10.02 V.

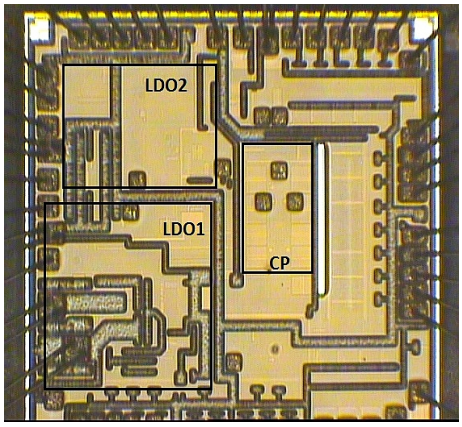


**Fig. 11.** The fabricated charge pump/LDO test chip.

In order to evaluate the effectiveness of correlating the capacitor in the oscillator to the pumping capacitors in the CP core, the corner simulations were repeated by replacing the oscillator capacitor with a low voltage capacitor. In both cases the output voltage of the CP was measured at 500 μA load. The oscillator frequency was also probed.

As expected,if the capacitors are not correlated the worst technological corner will be the one in which the specific capacitance for the low voltage capacitors is the highest (low oscillator frequency) and the specific capacitance for the pumping capacitors is the lowest. Correspondingly there is also a corner where the specific capacitance for the low voltage capacitors is the lowest (high oscillator frequency) and the specific capacitance for the pumping capacitors is the highest. In this corner the CP core will have the highest output voltage at the given 500 μA load.

**Table 1.**

| Simulation Results | Minimum Frequency [MHz] | Maximum Frequency [MHz] | Minimum Output Voltage at 500 μA load [V] | Maximum Output Voltage at 500 μA load [V] |
|---|---|---|---|---|
| Uncorrelated (different capacitor types) | 13.754 | 18.137 | 9.144 | 11.752 |
| Correlated (same capacitor type) | 13.25 | 18.68 | 10.02 | 10.84 |

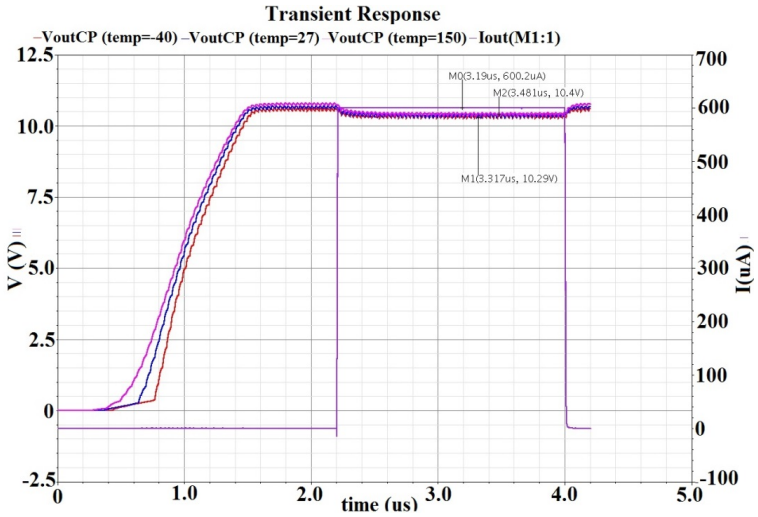


**Fig. 12.** Simulation results. Ramp up and load jump response at nominal supply voltage (4 V) at three different temperatures ($-40°$C, $27°$C, $150°$C).

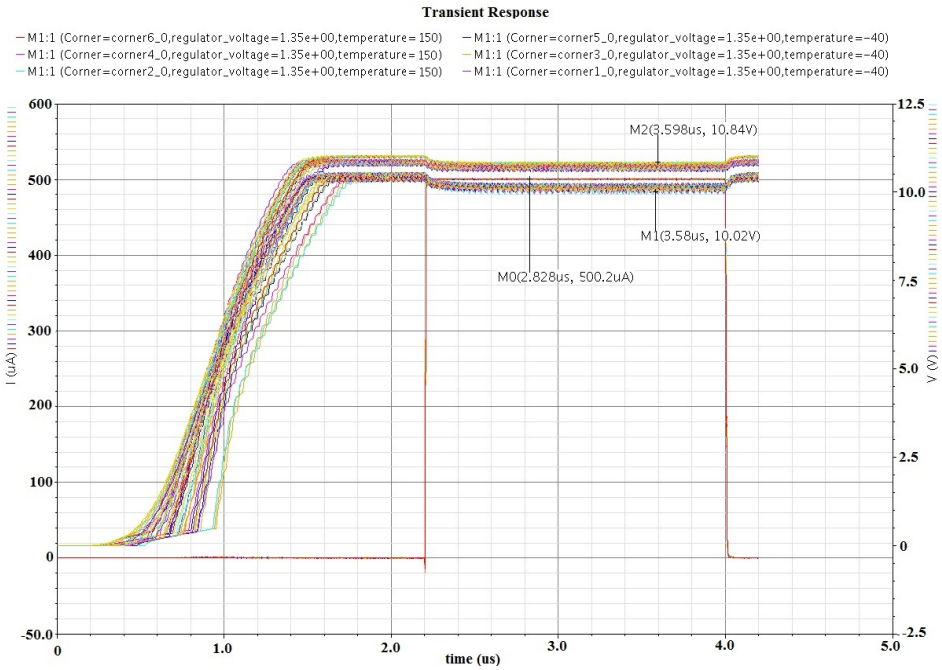


**Fig. 13.** Simulation results. Ramp up and load jump response in the relevant PVT (process voltage temperature) corners.

When the capacitors are correlated we can observe a much narrower spread of the

output voltage with process variations even if the frequency spread is of similar (or even slightly larger) magnitude.

In order to evaluate the pumping performance of the proposed topology versus existing circuits (described in [1], [5], [6]) output voltage versus load current simulations were performed. The schematics for the compared topologies are presented in Fig. 14 and the simulation results are depicted in Fig. 15. Diode-connected NMOS devices were used as passive switches for the classical Dickson CP (Fig. 14a). Besides the pumping capacitors, an additional (smaller) capacitor $C_X$ (Fig. 14b) is necessary for the implementation of Wu and Chang's CP described in [5] in order to provide the boosted voltage for the third charge transfer switch.

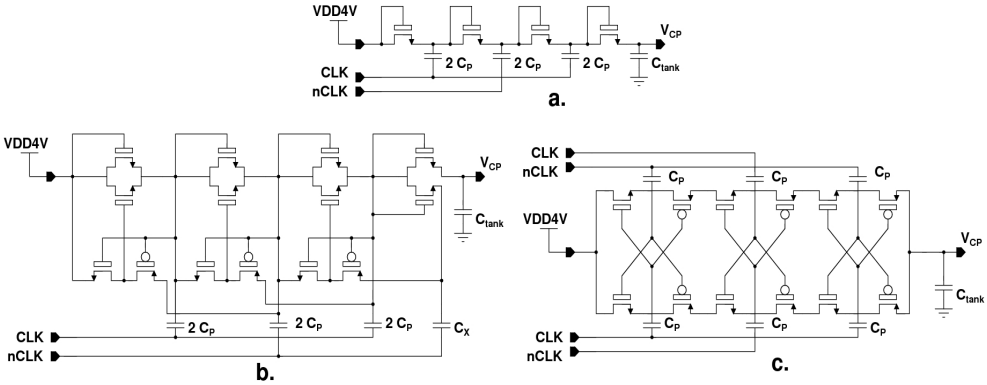


**Fig. 14.** Charge pump topologies used for comparison.
a) Dickson CP; b) CP proposed by Wu and Chang in [5];
c) CP proposed by Ming-Dou Ker, and Shih-Lun Chen in [6].

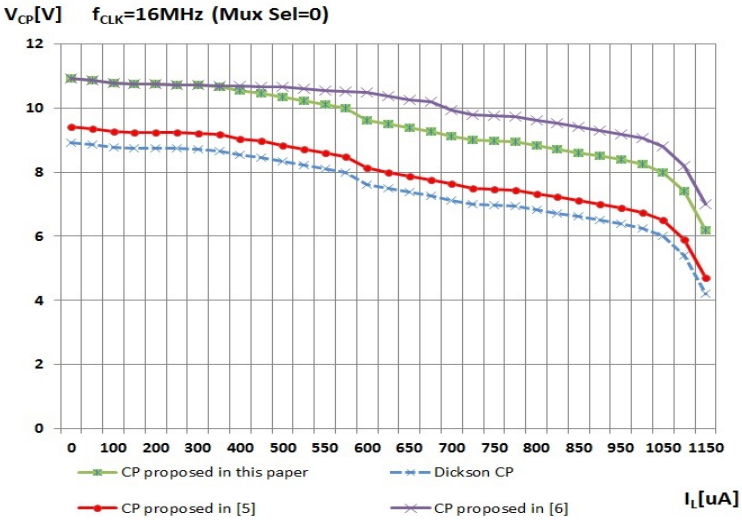


**Fig. 15.** Simulation results. Output voltage vs. load current for the proposed CP core vs. the original Dickson CP ([1]) and the topologies proposed in [5] and [6].

The same number of stages, clock frequency and supply voltage were considered for all the simulated CP circuits and the total pumping capacitance used was the same in each case. This means that for the topologies using only a single pumping chain ([1] and [5]) the pumping capacitors were double with respect to the proposed topology and the circuit presented in [6] which are using two pumping chains in parallel. This was done to ensure that any limitation in the current capability was not the result of insufficient pumping capacitance. In all cases ideal signal sources were used to drive the pumping capacitors. The simulations show that the pumping performance of the proposed topology is closer to the more complex architecture described by Ming-Dou Ker in [6]. This difference (in favor of Ming-Dou Ker's CP) is due to the lower charge transfer efficiency of the $ND_{1A}$, $ND_{1B}$ passive switches and is an accepted trade-off with circuit complexity.

### B. Test chip measurement results

Static measurements of the CP output voltage versus load current are presented in Fig. 16a (15.94 MHz clock provided directly by the internal oscillator when the selection bit for the multiplexer is 0) and Fig. 16b (with the CP core driven by the frequency-halved ∼7.97 MHz clock signal corresponding to the situation where only one LDO is active).

As expected, the measured CP output impedance is proportional to the clock frequency, approximately 2.103 KOhms for $f_{CLK}$=15.94 MHz and 4.254 KOhms for $f_{CLK}$=7.97 MHz. The maximum oscillator current drawn from the 1.5 V supply was found to be 78 µA while the maximum value for the CP ground current while sourcing 500 µA DC was measured at ∼2.8 mA. The supply voltages for the CP core as well as for the oscillator were generated on-chip by a dedicated internal regulator and were measured at approximately 4.05 V and 1.511 V respectively.

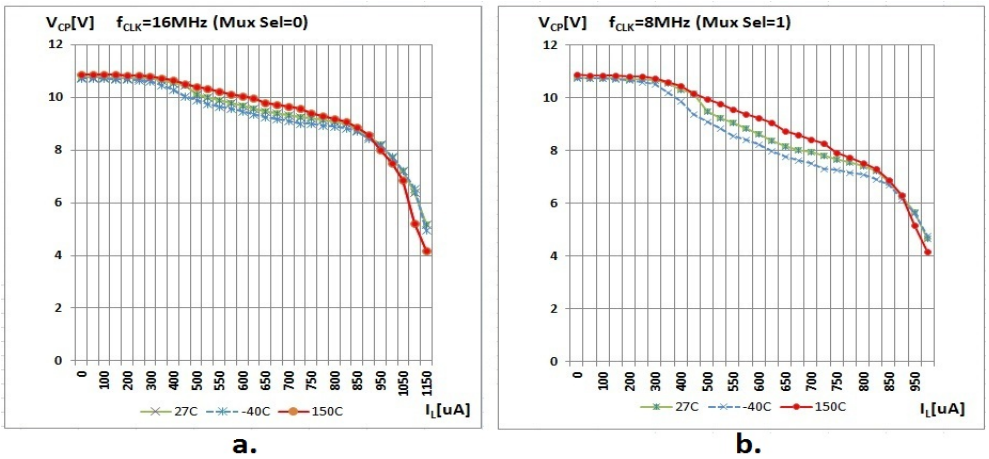


**Fig. 16.** a) Measured CP output voltage versus load current for $f_{CLK}$=15.94 MHz; b) Measured CP output voltage versus load current for $f_{CLK}$=7.97 MHz.

The characterization was done on three samples covering the full automotive temperature range [−40°C to 150°C]. Unfortunately because only three samples were measured, no statistical data related to the performance of the circuit is available.

Extracted PCM (process control monitoring) data shows that the measured samples were approximately in the nominal technological corner. Because there is a good agreement between simulations and measurements in the nominal corner, and the simulation models are mature, we also expect the statistical measurements to match the values obtained in the corner simulations.

## 4. Conclusion

A fully integrated dual-chain Dickson type charge pump making use of both active and passive charge transfer switches, optimized for sourcing DC current, was presented in this paper. The static measurements show that the current capability and output voltage are within specifications. By matching the type of capacitor used in the RC oscillator to the pumping capacitors in the CP core the output current capability variation was reduced. The CP core current consumption was also reduced by using improved drivers for the pumping capacitors.

# References

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