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On the Suppression of Output Oscillations in a Software Controlled DC-DC Buck Converter

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Abstract. In this paper unwanted output voltage oscillations due to the nonlinearities in a software controlled DC-DC Buck converter are analyzed and conditions for their suppression are given These conditions are correlated with the PID parameters designed using an algorithm that ensures imposed transient behavior for input steps and load variations.

Key words: DC-DC Buck converter, limit cycles, PID, describing function, ripples.

1. Introduction

In the last decade, there has been an increasing interest in using software capabilities for controlling DC-DC switching converters. Typically, a DC-DC switching converter consists of two main parts: an analog part that contains the switching devices an output filter and the load, and the second part, the feedback, that can be implemented using analog or software/ digital components. The use of software brings many advantages within the application, such as: configurability, flexibility and possibility to develop complex algorithms with low costs [1]–[3]. On the other hand, the use of software algorithms implemented in microcontrollers is limited by the computational speed and also by the finite resolution that is inherent for all mixed analog-discrete systems [4]–[6]. Both the quantization of the PWM generator block and the quantization of the ADC block are nonlinear effects that may cause

unwanted oscillations on the output voltage of the converter with the feedback loop closed. Various conditions for removing the limit cycles from the output voltage of DC-DC switching converters with software/digital control loop were presented in [6–9]. The nonlinear effects under study can be analytically modelled either by using describing function concept [9] or by writing down the nonlinear equations [7–8]. In this paper conditions to be satisfied by a DC-DC Buck converter with a PID controller in the feedback loop implemented in software to satisfy imposed performances and to prevent the presence of limit cycles on the output voltage are studied.

The paper is structured as follows. In Section 2 general aspects regarding the DC-DC Buck converter under study are presented. In Section 3 the ripples in the steady state behavior of the converter as well as the unwanted periodic oscillations associated with limit cycles are discussed. The linearized averaged model of the DC-DC Buck converter is presented in Section 4 together with analytical results regarding the presence of limit cycles on the output voltage. Simulation results are presented in Section 5 and Section 6 contains the conclusions of the study.

2. DC-DC Buck Converter – General Aspects

The application under study consists of a DC-DC Buck converter with the block diagram shown in Fig. 1.

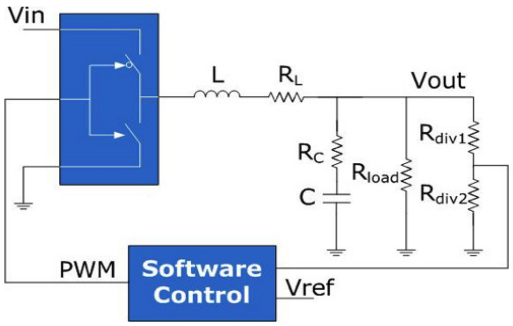


Fig. 1. DC-DC Buck Converter – Block Diagram.

For building up the DC-DC switching buck converter application an integrated circuit containing a half-bridge configuration and a driver for the MOSFETs is used. An internal block of the chip is responsible for creating two non-overlapping PWM signals to be applied to the switching devices, hence the presence of a single input port for the PWM control. For simplicity, only the on-resistances of the transistors are taken into consideration for simulation and for calculations. The chip operates in a wide input voltage range from 4.5 V to 45 V, with a maximum output current of 500 mA and a maximum PWM switching frequency of 500 kHz.

An LC low pass filter is connected at the output of the half bridge. The DCR (DC Resistance) of the output inductor – R_L and respectively the ESR (Equivalent Series

Resistance) of the output capacitor – R_C are considered, as shown in Fig. 1. For the current case study the output of the converter is a pure resistive load (R_{load}).

The mechanism for controlling the DC-DC Buck converter is implemented in software. For this purpose a microcontroller with the following features is used:

- Clock frequency: 80MHz;
- ADC resolution: 12 bits;
- ADC reference voltage: 3.3 V;
- PWM generation block: 2 PWM resolutions are available: 9 bits and 15 bits.

As shown in the block diagram from Fig. 1, a resistor divider is used in order to adjust the level of the output voltage to the maximum allowed value on the ADC input (3.3 V). Inside the microcontroller a PID algorithm is implemented. The PID parameters have been tuned aiming good transient performances: overshoot values less than 10%, settling time less than 200 μs, steady state value of 5 V and maximum steady state error of ±5%. These performances are desired to be obtained for different line steps and load steps scenarios. For the current case study two test scenarios are analyzed:

- Input step scenario from 8 V to 13 V, at a constant load current of 10 mA;
- Load step scenario from 10 mA to 300 mA, at a constant supply voltage of 18 V.

The models used for simulations are implemented in Matlab/Simulink with components from Simscape library.

3. DC-DC Buck Converter – Ripples Vs. Limit Cycles

The output voltage of a DC-DC converter in steady-state can exhibit not only ripples but also unwanted limit cycles. The oscillations that appear on the output voltage in steady state determined by the PWM switching activity are called ripples, while the ones determined by the nonlinearities present in the system are known as limit cycles [6]. The output voltage ripples are determined by the charging and discharging cycles of the capacitor, therefore the amplitude and the frequency of these oscillations are well defined. On the contrary, the amplitude and the frequency for the limit cycle oscillations are difficult to be determined as they are produced by nonlinear effects.

Moreover, the values of the output filter components are chosen based on the desired values for the output voltage ripple, Δv_C, and inductor current ripple, Δi_C, using the following two expressions [10]:

$$\Delta v_C = \frac{\Delta i_L}{8 \cdot f_{pWM} \cdot C} + \Delta i_L \cdot R_C, \tag{1}$$

$$\Delta i_L = \frac{(V_{in} - V_{out}) \cdot D}{L \cdot f_{PWM}}, \tag{2}$$

where: Δv_C – output voltage ripple; Δi_L – inductor current ripple; f_{PWM} – PWM frequency; D – duty cycle of the PWM signal; R_C – ESR of the output capacitor; L – output inductor; C – output capacitor; V_{in} – input voltage of the DC-DC converter; V_{out} – output voltage of the DC-DC converter.

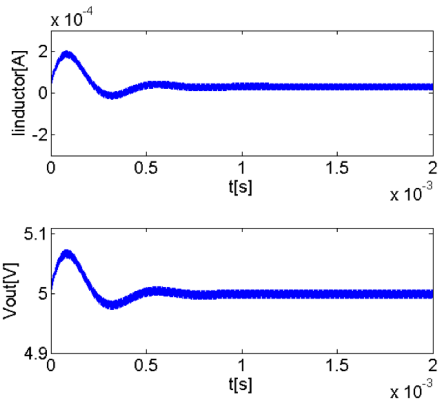
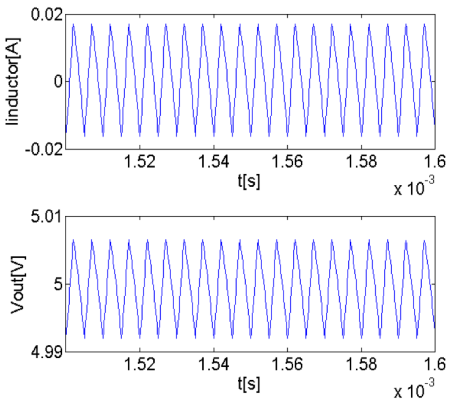
The values chosen for the output filter components designed to get a maximum inductor current ripple of 150 mA and a maximum output voltage ripple of 50 mV are presented in Table 1:

Table 1. DC-DC Buck Converter – Output Filter Components

Parameter	**Nominal value**	**Tolerance**
L	220 uH	$\pm$ 5%
R_L	1 Ω	$\pm$ 10%
C	22 uF	$\pm$ 20%
R_C	0.21 Ω	$\pm$ 10%

Open loop simulation results showing the amplitude of the ripples of the output voltage and of the inductor current, are presented in Table 2.

Table 2. DC-DC Buck Converter – Open Loop Simulation

Open loop simulation results	Zoom on simulation results
	

The simulation was performed keeping the input voltage at 13 V, while the output current is 10 mA. Table 3 compares the results obtained from simulations and from calculations regarding the values of the output voltage ripple and respectively for the inductor current ripple. It can be seen that the results fit very well.

Table 3. Values for the output voltage and inductor current ripples

Ripples	Equations	Simulations
Δv_C [mV]	16.65	15
Δi_L [mA]	69.9	68.4

A PID set used in the feedback loop is considered to be optimal when the output voltage of the converter is stable and satisfies specific transient performances for different load step and line step scenarios. Moreover the steady state output voltage should be characterized only by ripples with amplitude lower than the one used for dimensioning the output filter components as described above. The presence of the limit cycles on the output voltage of the converter can be pointed out by performing closed loop simulations with different PID settings as shown in Fig. 2. The test scenario considered for the simulation is a line step from 8 V to 13 V at a constant load current of 10 mA.

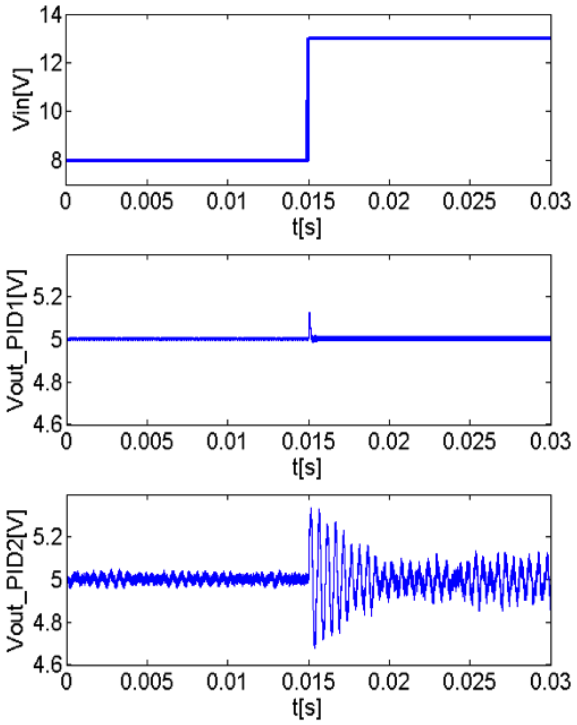


Fig. 2. DC-DC Buck converter - Closed loop simulation.

It can be seen that in the first case the output voltage of the converter is characterized only by ripples, while in the second case limit cycle oscillations are present.

Moreover, because of the poor choice of the PID pair (very close to the stability border), the amplitude of the limit cycles is very high, reaching values 20 times higher than the desired ripples. Therefore it is very important to be able to tune the control loop such that no limit cycles would be present at the output voltage of the converter.

4. Conditions for Removing Limit Cycles – Theoretical Aspects

4.1. Limit cycles - Theoretical aspects

As already shown, limit cycles are unwanted periodic oscillations that appear on the output voltage of the DC-DC Buck converter due to the nonlinearities present in the system.

Reference [6] proposes a set of conditions that the system should satisfy in order to remove the limit cycles from the output voltage:

1. The feedback path must contain a positive integral term:
$$K_i > 0 \tag{3}$$
2. The resolution of the PWM generation block should be higher than the resolution of the ADC block:
$$Res_{PWM} > Res_{ADC} \tag{4}$$
3. The characteristic equation of the closed loop transfer function when the describing function of the nonlinear block (N(A)) is also taken into consideration should be nonzero, for all $A > 0$ and in the entire range of frequency:
$$1 + N(A) \cdot T(j \cdot \omega) \neq 0, \forall A > 0, \forall \omega > 0. \tag{5}$$

In the following, the above conditions are discussed in relation to the current application and then used for tuning the PID parameters.

4.2. Describing function – Theoretical aspects

A describing function approximates a non-linear system with a linear time-invariant transfer function that depends on the amplitude of the input signal [11]. Considering that at the input of a nonlinear block, a sine wave of amplitude A is applied, then the amplitude and phase shift of the fundamental component of the output signal will depend on A. Let $x(t) = A \sin \theta$ be the input signal applied to the considered nonlinear block. Then the output signal can be represented using the Fourier series as:

$$y(t) = h_1 \sin \theta + h_2 \cos \theta + ... \tag{6}$$

The coefficients of the Fourier series can be determined using the following expressions:

$$h_1 = \frac{1}{\pi} \cdot \int_0^{2\pi} f(A \cdot \sin\theta) \sin\theta \mathrm{d}\theta, \tag{7}$$

$$h_2 = \frac{1}{\pi} \cdot \int_0^{2\pi} f(A \cdot \sin\theta) \cos\theta \mathrm{d}\theta. \tag{8}$$

Once these coefficients are determined, the describing function can be determined using the following equation:

$$N(A) = \frac{h_1^2 + h_2^2}{A} \cdot e^{j \cdot \left(atan\left(\frac{h_1}{h_2}\right)\right)}. \tag{9}$$

For the DC-DC Buck converter application, two quantization blocks are present within the application: one for the ADC block and one for the PWM block. In order to avoid the presence of limit cycles on the output voltage of the converter, the PWM block should have a resolution with at least 1 bit higher than the resolution of the ADC block. In this case, the quantization from the ADC becomes the critical one, therefore only the describing function of the ADC quantizer will be taken into consideration when determining the characteristic equation of the closed loop system.

The describing function of the ADC quantizer, determined based on the equations (6)–(9) are:

$$N(A) = \begin{cases} 0,\ 0 < A < \dfrac{\delta}{2} \\ \dfrac{4 \cdot \delta}{\pi \cdot A} \cdot \displaystyle\sum_{i=1}^{n} \sqrt{1 - \left(\frac{2 \cdot i - 1}{2 \cdot A} \cdot \delta\right)^2},\ \dfrac{2 \cdot n - 1}{2} \cdot \delta < A < \dfrac{2 \cdot n + 1}{2} \cdot \delta \end{cases} \tag{10}$$

where δ represents the quantization step and n is a variable that is used to define the interval between two consecutive quantization steps that contains the amplitude of the input signal.

The graphical representation of this describing function is given in Fig. 3, where the maximum value of the function $4/\pi$ is highlighted.

5. DC-DC Buck Converter – Linearized Averaged Model

In order to express the third condition mentioned in section 3, the loop transfer function of the DC-DC Buck converter is needed. The linearized averaged model of the system is extracted as presented in [12]. Three transfer functions are of interest for this system:

- Input-to-Output transfer function - captures the behavior of the system when the input voltage of the converter is changed;
- Control-to-Output transfer function – describes the change in the output voltage when the duty cycle of the PWM signal is changed;

- Output impedance – characterizes the system when a change in the load current is present in the system.

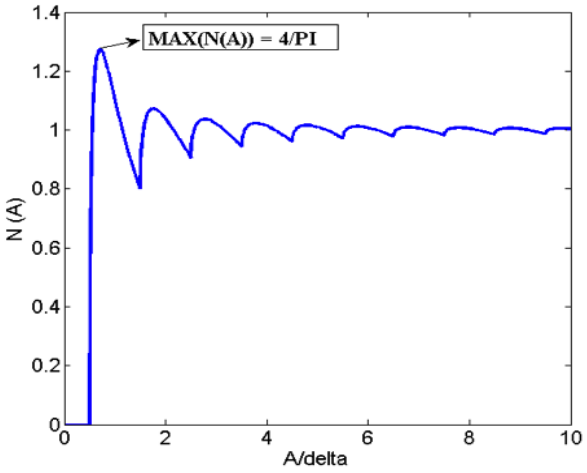


Fig. 3. Describing function for the ADC quantizer.

The open loop transfer functions in the analog domain extracted using the approach presented in [12] are:

- Input-to-Output transfer function in open loop:

$$H_{in\_out\_openloop}(S) = \frac{H_{in\_out\_0} \cdot \left(1 - \frac{s}{\omega_{z1}}\right)}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q \cdot \omega_0} + 1} \tag{11}$$

- Control-to-Output transfer function in open loop:

$$H_{ctrl\_out\_openloop}(S) = \frac{H_{ctrl\_out\_0} \cdot \left(1 - \frac{s}{\omega_{z1}}\right)}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q \cdot \omega_0} + 1} \tag{12}$$

- Output Impedance in open loop:

$$Z_{out\_openloop}(S) = \frac{Z_{out\_0} \cdot \left(1 - \frac{s}{\omega_z}\right)\left(1 - \frac{s}{\omega_{z1}}\right)}{\left(\frac{s}{\omega_0}\right)^2 + \frac{s}{Q \cdot \omega_0} + 1} \tag{13}$$

where:

$$H_{in\_out\_0} = \frac{D \cdot R_{load}}{R_{load} + (rds_{on} + R_L)}$$

$$H_{ctrl\_out\_0} = \frac{Vin \cdot R_{load}}{R_{load} + (rds_{on} + R_L)}$$

$$Z_{out\_0} = -\frac{R_{load} \cdot (rds_{on} + R_L)}{R_{load} + (rds_{on} + R_L)}$$

$$\omega_0 = \sqrt{\frac{R_{load} + rds_{on} + R_L}{L \cdot C \cdot (R_{load} + R_C)}}$$

$$Q = \frac{\sqrt{R_{load} + rds_{on} + R_L} \cdot \sqrt{L \cdot C \cdot (R_{load} + R_C)}}{(rds_{on} + R_L) \cdot C \cdot (R_{load} + R_C) + C \cdot R_{load} \cdot R_C + L}$$

$$\omega_{z1} = -\frac{1}{R_C \cdot C}, \quad \omega_z = -\frac{rds_{on} + R_L}{L}.$$

The system under study is a mixed analog-discrete system. To determine the closed loop transfer function of the DC-DC Buck converter controlled by a PID algorithm implemented in software, we chose to work in the discrete domain. In order to do this, the discrete versions of the open loop transfer functions (11) – (13) are first determined using the ZOH transform [13]. After applying the analog-to-discrete transform, the closed loop transfer functions can be determined:

- Input-to-Output transfer function in closed loop:

$$H_{in\_out\_closedloop}(z) = \frac{H_{in\_out\_openloop}(z)}{1 + T(z)} \tag{14}$$

- Reference-to-Output transfer function in closed loop:

$$H_{ref\_out\_closedloop}(z) = \frac{1}{K_{ADC} \cdot K_{sensor}} \cdot \frac{T(z)}{1 + T(z)} \tag{15}$$

- Output Impedance in closed loop:

$$Z_{out\_closedloop}(z) = \frac{Z_{out\_openloop}(z)}{1 + T(z)}. \tag{16}$$

where:

$$T(z) = K_{sys} \cdot H_{ctrl\_out}(z) \cdot H_{delay}(z) \cdot H_{PID}(z),$$

$$K_{sys} = K_{PWM} \cdot K_{ADC} \cdot K_{Sensor},$$

$$H_{PID}(z) = K_P + K_i \cdot \frac{1}{1 - z^{-1}} + K_d \cdot \left(1 - z^{-1}\right),$$

$$H_{delay}(z) = z^{-1},$$

$$K_{PWM} = \frac{1}{MaxDutyCycleValue},$$

$$K_{ADC} = \frac{\left(2^{adc\_res} - 1\right)}{V_{adc\_ref}},$$

$$K_{Sensor} = \frac{R_{div2}}{R_{div1} + R_{div2}}.$$

The choice of working in the discrete domain leads to the following modification of the condition specified in equation (5):

$$1 + N(A) \cdot T\left(e^{j \cdot \omega \cdot T_{PWM}}\right) \neq 0, \ \forall A > 0, \ \forall \omega > 0 \tag{17}$$

6. Results And Discussion

A. Condition 1

First condition is satisfied because the integral term used for the PID controller is always greater than zero.

B. Condition 2

In Section 2 the features of the microcontroller used in the feedback loop of the converter were presented. The resolution of the ADC block is 12 bits, while for the generation of the PWM, the user can choose between using the 9 bits or the 15 bits resolution.

In the following tables, simulation results for both 9 bits and 15 bits PWM resolution are presented, for two different configurations of the PID block in case of a line step scenario from 8 V to 13V with a constant load current of 10 mA [14]. The first considered PID configuration is: $K_p = 0.571$; $K_i = 0.034$; $K_d = 5.212$, while the second one is: $K_p = 2.328$; $K_i = 0.176\, K_d = 16.941$.

The simulation results presented in Table 4 show the fact that by increasing the PWM resolution from 9 bits to 15 bits, the limit cycle oscillations do not appear on the output voltage of the converter when the first configuration of the PID parameters is used. However for the second PID configuration the limit cycle oscillations are still present at the output voltage after increasing the resolution of the PWM block (see Table 5).

From the above plots, it follows that satisfying the first two conditions is necessary but not sufficient for removing the limit cycles from the output voltage of the DC-DC Buck converter.

Table 4. Increased PWM resolution – First PID pair – Input Step Scenario

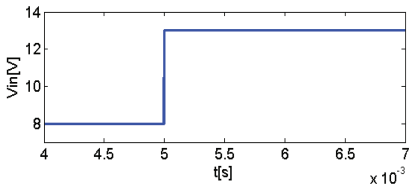
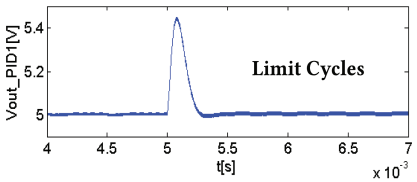
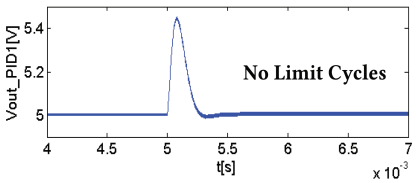
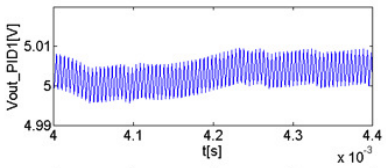
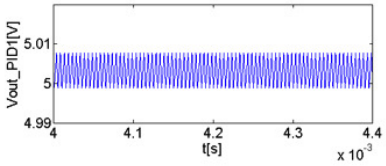
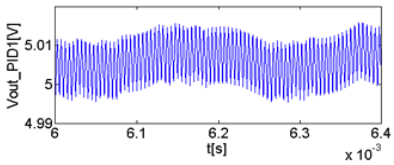
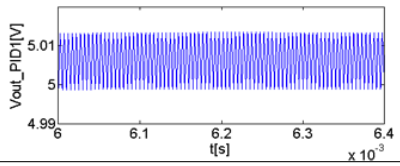
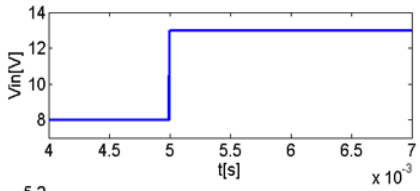
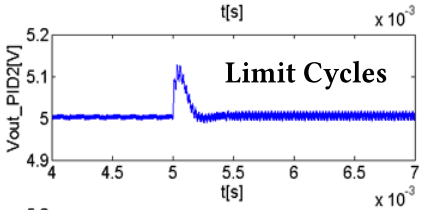
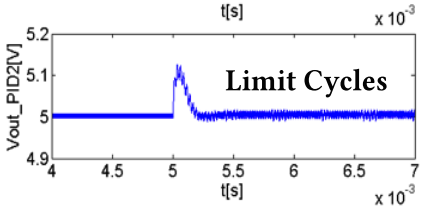
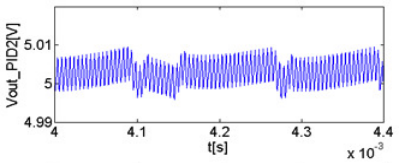
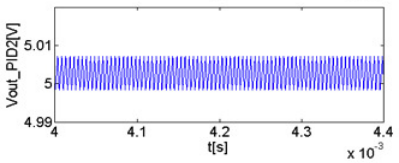
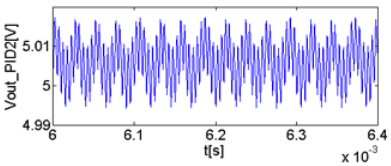
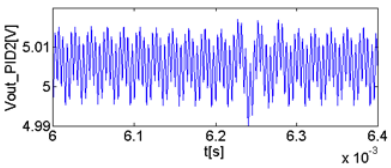
Input Step from 8 V to 13 V	
PWM Resolution 9 bits	
PWM Resolution 15 bits	
Zoom on the steady state before the input step	
PWM Resolution 9 bits	
PWM Resolution 15 bits	
Zoom on the steady state after the input step	
PWM Resolution 9 bits	
PWM Resolution 15 bits	

Table 5. Increased PWM resolution – Second PID pair – Input Step Scenario

Input Step from 8 V to 13 V	
PWM Resolution 9 bits	
PWM Resolution 15 bits	
Zoom on the steady state before the input step	
PWM Resolution 9 bits	
PWM Resolution 15 bits	
Zoom on the steady state after the input step	
PWM Resolution 9 bits	
PWM Resolution 15 bits	

C. Condition 3

The third condition for removing limit cycle oscillations from the output voltage is used in the discrete version presented in equation (17). For applying it on the DC-DC Buck converter, the closed loop transfer functions in the discrete domain derived in Section 4 are used.

In order to analytically predict if limit cycle oscillations will be present or not on the output voltage of the converter, the characteristic equation from (17) is set to 0 and the following system of equations is solved:

$$\begin{cases} 1 + Re\left\{N\left(A\right) \cdot T\left(e^{j \cdot \omega \cdot T_{PWM}}\right)\right\} = 0 \\ Im\left\{N\left(A\right) \cdot T\left(e^{j \cdot \omega \cdot T_{PWM}}\right)\right\} = 0 \end{cases} \tag{18}$$

where $N(A)$ and ω are considered unknown.

If the system of equations (18) has real solutions, then the value of $N(A)$ is compared with $4/\pi$ which is the maximum value of the describing function for the ADC quantizer (Fig. 3). If the determined $N(A)$ is higher than $4/\pi$ then the output voltage will be characterized only by ripples, because the graphical representation of the describing function (Fig. 3) and the wanted value for $N(A)$ have no intersection point. If the value calculated for $N(A)$ is lower than $4/\pi$, then the output voltage will exhibit limit cycle oscillations with an angular frequency equal to ω.

At first the above described approach will be used in order to analytically predict the presence of the limit cycles on the output voltage for the two considered PID configurations presented in Section 6B.

Since the two examples focused on a test scenario of input step from 8 V to 13 V, keeping a constant load current of 10 mA, condition (18) should be applied after determining the closed loop transfer functions that characterizes the two different operating points of the system: the first one corresponding to the initial value of the step and the second one corresponding to the final value of the step. Considering that the first two conditions are satisfied, only the case with 15 bits PWM resolution is of interest.

The results for the first configuration of the PID block are analyzed. For each operating point the real solutions for the system of equation (18) are determined:

- Operating point before applying the step:

$$N\left(A\right) = 6.03 \tag{19}$$

- Operating point after applying the step:

$$N\left(A\right) = 3.71 \tag{20}$$

It can be seen that for both operating points the obtained values are higher than the maximum value of the describing function of the ADC quantizer (Fig. 3). This means that for all positive values of A and ω, the characteristic equation defined in (17) is different of 0. Thus, the third condition is satisfied, therefore the output voltage

will present no limit cycle oscillations. The simulation results (Table 4) confirm the theoretical results.

The spectrum of the output voltage can offer an intuitive image on the composition of the output signal. Table 6 presents the magnitude spectrum of the output voltage of the converter after the input step is applied and when the first PID configuration is used:

Table 6. DC-DC Buck Converter – Spectrum of the output voltage – First PID configuration

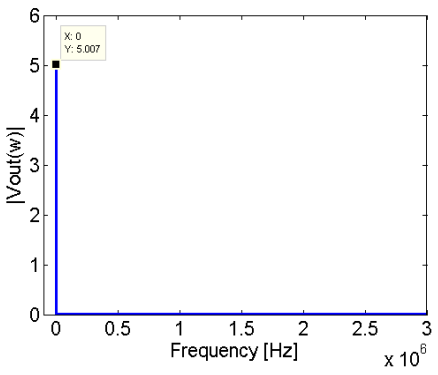
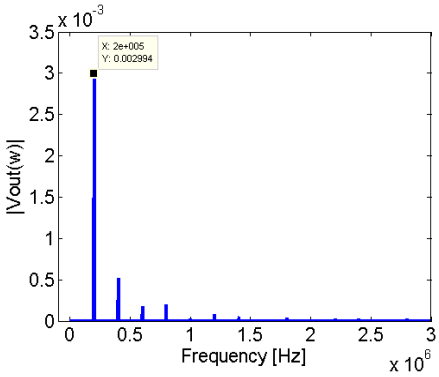
Spectrum of the output voltage signal	Zoom in – Spectrum of the output voltage signal
	

Table 6 shows that, in this case, the spectrum of the output voltage is composed of a 5 V DC component and additional spectral components placed at frequencies which are multiple of the PWM frequency.

The same approach is applied for the second PID configuration. The values obtained for the describing function for each operating point are:

- Operating point before applying the step:

$$N(A) = 1.81 \tag{21}$$

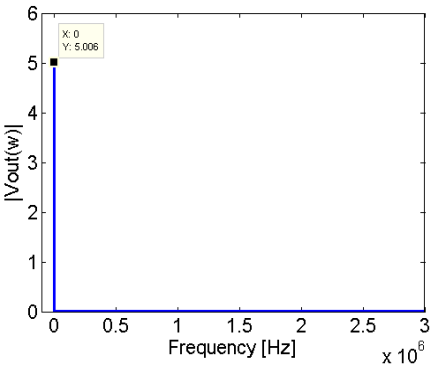
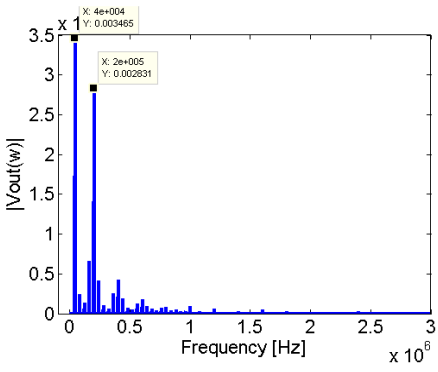
- Operating point after applying the step:

$$N(A) = 1.119; \quad \omega = 242363 \frac{rad}{s} \rightarrow f_{limit\_cycle} = 38.57\,\text{kHz} \tag{22}$$

For the first operating point, the value is higher than the maximum value of the ADC describing function of $4/\pi$, while for the second operating point the value is less than this value. This means that it exists an amplitude $A > 0$ and a pulsation $\omega > 0$, for which the characteristic equation (17) is zero. In this case, the third condition is not satisfied, therefore the output voltage will present limit cycle oscillations. The simulation results confirm the theoretical results.

For the second PID configuration, the magnitude spectrum of the output voltage of the converter, after the input step, is presented in Table 7:

Table 7. DC-DC Buck Converter – Spectrum of the output voltage - Second PID configuration

Spectrum of the output voltage signal	Zoom in – Spectrum of the output voltage signal
	

In this case, the spectrum of the output voltage contains also an additional spectral component placed at a frequency of 39 kHz, which is in fact the limit cycle frequency predicted analytically in equation (22).

D. Tuning the PID coefficients

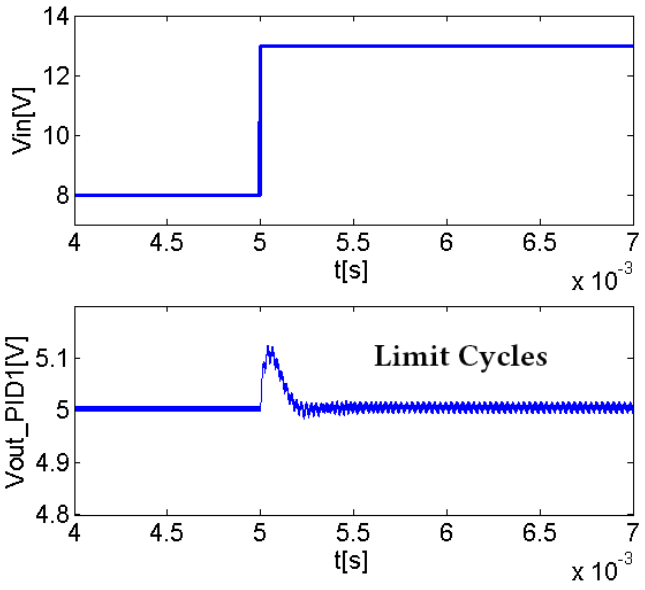
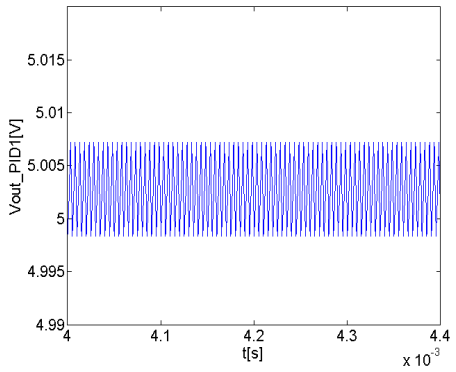
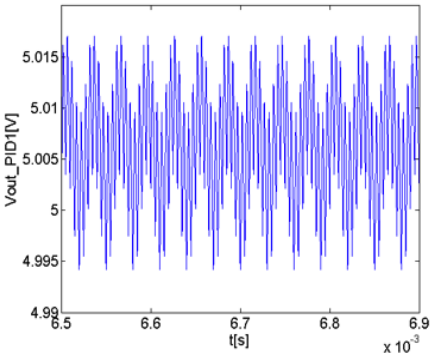
An algorithm for tuning the PID parameters was implemented in order to obtain the following transient performances for the output voltage: steady state error less than 5%, overshoot value less than 10%, settling time value less than 200 µs. The algorithm uses the discrete transfer functions presented in section 5 and the main idea is to search for the optimum locations of the discrete poles such that the step response satisfies the imposed specifications. First the dominant poles are determined considering a second order transfer function prototype and then an adaptive searching algorithm is applied in order to determine the optimum locations for the rest of the poles such that the performances are satisfied and a set of real positive PID parameters are obtained.

This algorithm is applied first for the input step scenario from 8 V to 13 V, at a constant load current of 10 mA, and then for the load step scenario from 10 mA to 300 mA at a constant input voltage of 18 V.

The resulted PID set after applying the algorithm for the input step scenario is: $K_p = 191.2$; $K_i = 14.49$; $K_d = 1391.29$, while for the load step scenario the value for the PID parameteres are: $K_p = 120.69$; $K_i = 9.2$; $K_d = 872.31$. The corresponding waveforms for the output voltage are given in Table 8.

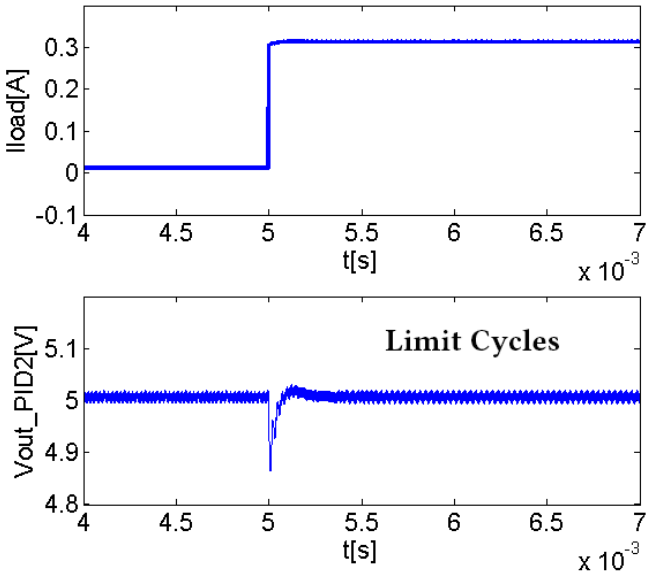
From Table 8 it can be seen that in both cases, limit cycle oscillations are present on the output voltage of the converter.

Table 8. Results of tuning the PID – Original Algorithm

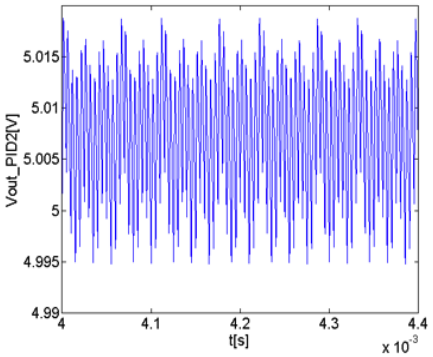
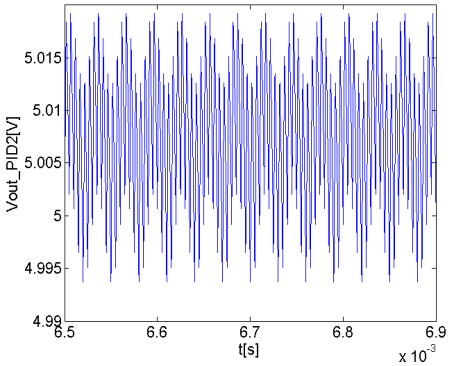
Input Step Scenario	
$K_p = 191.2;\ K_i = 14.49;\ K_d = 1391.29$	
	
Zoom on the steady state	
Before the step	After the step
	

Load Step Scenario

$K_p = 120.69;\ K_i = 9.2;\ K_d = 872.31$



Zoom on the steady state

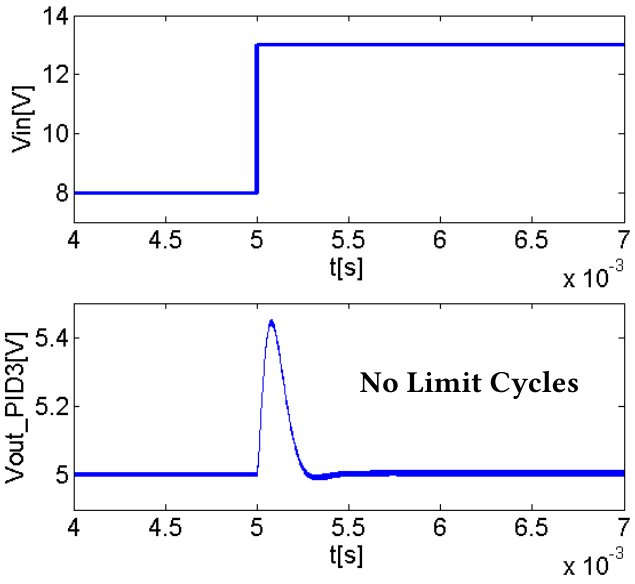
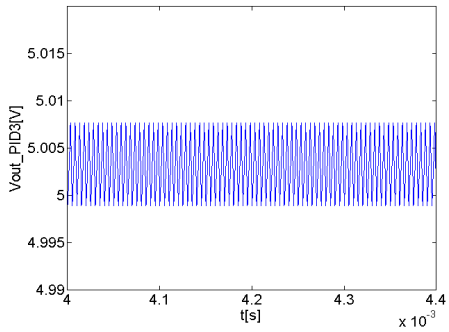
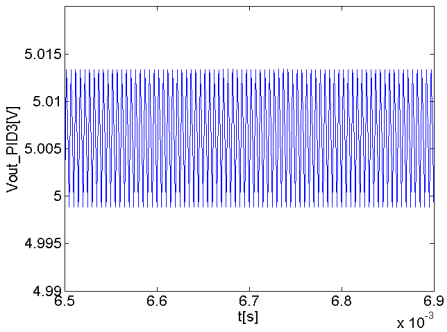
Before the step	After the step
	

The algorithm described above took into consideration only the desired transient performances of the converter. No limitations regarding the steady state behavior were imposed so far.

The algorithm was next modified in order to take into account also the condition for removing the limit cycles provided by equation (17). So in the searching

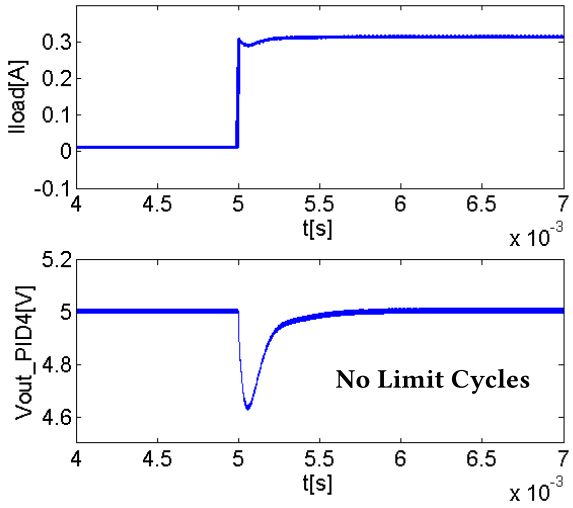
algorithm additional constraints were imposed for the PID parameters such that the characteristic equation of the closed loop transfer function of the system should be always different than zero. If more than one PID set satisfies the constraints, then the algorithm chooses the one that offers maximum value for the N(A) parameter. Table 9 shows the new PID sets for both the input step scenario and load step scenario and also the waveforms resulted for the output voltage.

Table 9. Results of tuning the PID – Modified Algorithm

<table>
<tr><td colspan="2">Input Step Scenario</td></tr>
<tr><td colspan="2">$K_p = 46.9;\ K_i = 2.8;\ K_d = 428.03$</td></tr>
<tr><td colspan="2"> 
</td></tr>
<tr><td colspan="2">Zoom on the steady state</td></tr>
<tr><td>Before the step</td><td>After the step</td></tr>
<tr><td> 
</td><td> 
</td></tr>
</table>

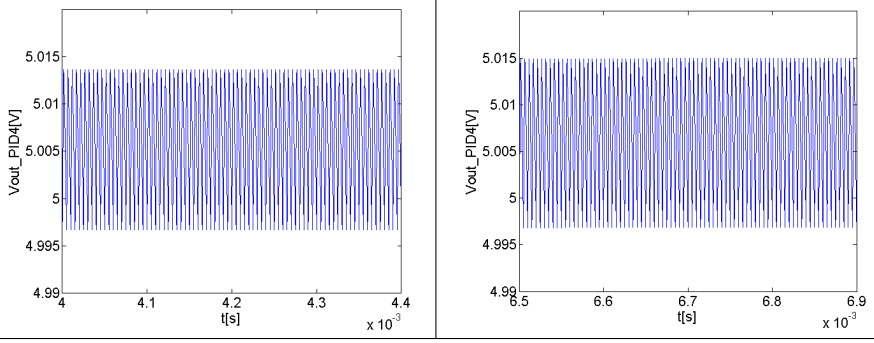
Load Step Scenario

$K_p = 11.34;\ K_i = 0.36;\ K_d = 142.34$



Zoom on the steady state

Before the step	After the step



From the above table, it can be seen that the modified algorithm can provide PID values for which the transient performances are satisfied but also the steady state of the output voltage has no limit cycles.

7. Conclusions

We have analyzed the conditions that a DC-DC Buck converter with software control loop should satisfy in order to avoid nonlinear output voltage oscillations.

Based on these conditions a tuning algorithm was developed in order to obtain desired transient performances as well. The algorithm has been built using a combination of constraints based on linear (dominant pole allocations) and nonlinear (describing function) control theory. Simulation and experimental results confirm the validity of theoretical considerations.

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