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Investigation of 60 GHz LNA with estimated S11 values based on mathematical model and numerical solution

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Abstract. This paper presents the design of a millimeter-wave low noise amplifier (LNA) realized using a 0.13 μm silicon germanium bipolar complementary metal oxide semiconductor process technology. The effect of input matching on an LNA is investigated. A small-signal equivalent circuit, which depicts the resistor-inductor-capacitor relationship of the input impedance network, is explored to determine its input impedance. A MATLAB code was written to understand the frequency response of the input matching network. The responses obtained are expected to be applied to the LNA to determine the input reflection coefficient ($\mid S_{11} \mid$). The equivalent circuit model (ECN) is verified numerically using 2D Advanced Design System (ADS) software. Thereafter, a step-by-step methodology that can be applied in realizing a 60 GHz LNA at the V-band is formulated. The amplifier is designed using lumped elements in a two-stage cascode topology based on a novel matching network. The matched network consists of an L-input and a T-output matching network as well as inductive emitter degeneration. The output network is designed to enhance maximum power transfer, whereas inter-stage matching is designed to optimize for high gain while minimizing the noise of the local area network. The transistor configuration is implemented by varying the length of the transistor to observe the minimal noise figure and the maximum gain, while keeping the voltage across the collector, emitter and the base constant. By utilizing the cascode topology and series peaking inductor, ($\mid S_{11} \mid$) of the LNA

peaks at 14 dB, whereas the output reflection coefficient (| S_{22} |) achieved is 25 dB. The estimated value of S11 using the ECN was about 12 dB. The noise factor is 4.3 dB minimum at 60 GHz, whereas the forward gain (| S_{21} |) of the LNA is well above 26 dB.

Keywords: optimal current density; inductive degenerative emitter, cascode topology; S-parameters; LNA; input matching; parasitic capacitance; common-emitter; millimeter-wave; input reflection coefficient.

1 Introduction

Research interest in the millimeter-wave (mm-wave) frequency and the development of an integrated circuit at the 60 GHz frequency range can be attributed to many factors, among others 7 GHz bandwidth typically available between 56 and 64 GHz, coupled with the high data rate that can be experienced by end users on the dense and short-range wireless network. This is also expected to reduce pressure on the low frequency, eventually releasing originally allocated spectrum for other uses. The earlier suggested demerit of the system, the short-range coverage, potentially offers additional strength to the frequency range, as it is secured against interference from other signals. An added benefit realized from the 60 GHz frequency is the development of miniaturized circuitry using III-V semiconductors, complementary metal oxide semiconductor (CMOS) and heterojunction bipolar transistor (HBT) technologies. The scaling down of these manufacturing technological nodes over the last four decades, currently to a 10 nm process, affords the opportunity for more development, as predicted by Moore's law [1]. Because of the low quality factor associated with passive components, and parasitics that limit the frequency of operation [2] (above 10 GHz) evident in the mm-wave frequencies, designing of an integrated circuit (IC) is a challenging task. Likewise, the importance of achieving a low noise figure (NF) and high gain in the low noise amplifier (LNA) makes it even more rigorous. Lumped elements used in designing LNA have become less appropriate at the mm-wave frequency, since the desired characteristics of the lumped element vary in response to the electromagnetic effect, thus leading to the use of transmission lines. Critical performance parameters, such as impedance matching, gain and the noise factor, must be considered while designing an LNA. Input impedance matching ensures maximum power transfer, low degradation of NF and a reduction in signal losses between the source impedance and the output. The choice of any matching topology is determined by complexity in implementation, adjustability and bandwidth range [3].

In selecting the bias approach for the LNA, reducing the direct current (dc), power consumption and total NF of the LNA circuit must be the overall end goal. In [4], traditional current reuse topology is employed to share current across two common-source (CS) transistors: a small-signal grounded CS transistor and an emitter degenerated CS transistor. The supply current is shared across the transistor. In [5], a two-stage cascode topology using a 40 nm CMOS process was designed with the goal of reaching the minimum NF at the first stage. The common-gate, CS and series inductor between the two transistors was optimized for this purpose. In [6], current reuse sources are arranged in a current-sharing mode offering 50% power sharing, connecting across each cascode stage while increasing its gain. Employing this approach requires the connection of a capacitor and an inductor between the base of transistor Q_2 and the collector of transistor Q_1 is a pathway for the reuse of current in the circuit with a supply voltage V_{DD}. The capacitor provides an ac short in series, which is an independent and alter-

nate path for biasing the LNA. The design methodology of a broadband (47–67 GHz) LNA was discussed in [7]. Wideband input matching was realized by using the source degenerative emitter at mm-wave frequencies. A T-matching network is employed at both the input matching network (IMN) and output matching network (OMN) of the LNA [8, 9] to ensure wide bandwidth, high power gain and low NF at the frequency of interest. An effort was made to design the LNA in the first two stages of LNA [9] with optimal noise matching. Likewise, a D-band LNA, implemented in a 130 nm silicon germanium (SiGe) BiCMOS technology, consisting of two cascode topology stages terminated inductively at the base, was reported in [10]. A bias circuit, made of a current mirror and resistors, is utilized to regulate the flow of current in the circuit. The termination at the base using an inductor was aimed at increasing the gain at the frequency of interest. While in [10, 11], T-section matching is utilized at both the IMN and OMN, a CS topology is used as the first stage and a cascode topology forms the second stage [10]. Similarly, a three-stage differential LNA is designed using a transmission line in [11]; the first two stages are aimed at optimum noise matching and the last is conjugate matched to ensure maximum power transfer. Even though the process technology employed in [12] is similar to that used in this paper, an inductive base is seen on the common-base (CB) transistor as part of a two-stage cascode topology specifically aimed at boosting gain.

This work examines the contribution of parasitics from the active component in the transistors and passives, on the input impedance matching, while showing the estimated input return loss, S_{11}, via mathematical analysis. On completing this, the design methodology employed in the design of a 60 GHz LNA is described. The paper is organized as follows: In Section 2, the design theory for the input matching, utilizing its small-signal analysis based on the common-emitter (CE) configuration, is derived and explained. Furthermore, relevant equations are formulated, derived, discussed and modeled. In Section 3, the design methodology for the design of the LNA is outlined. A single-stage cascode with a series peaking inductor across the CE and CB transistors is used for this analysis. The circuit schematic describing the approach used for the 60 GHz LNA is described in Section 4. The results and discussion are presented in section 5 and lastly, the conclusion is presented in Section 6.

2 Design Methodology of Input Matching Using Mathematical Analysis

The IMN and OMN are fundamental to the performance of the LNA. However, the IMN offers a distinctive function as it controls the overall NF of the LNA. In this design, a simple resistor-inductor-capacitor circuit using a common-emitter configuration with inductive degeneration is deployed in the IMN of the 60 GHz LNA, as shown in Figure 1, while an equivalent circuit of the input matching is depicted in Figure 2. $C_{pad}, C_{bc}, C_{be}, l_e, l_b$ and R_e are modeled mathematically and subsequently used in determining the frequency response of the IMN. The resistance R_e is resistance associated with the inductor, l_e, which is implemented to balance the real part of the input matching. The pad capacitance, C_{pad}, is connected in parallel to the reflected parasitic capacitance in the base-collector junction, C_p. C_{pad} is incorporated as part of the matching network.

The addition of l_e and l_b introduces an imaginary input matching component to the circuit. l_b is assumed as an ideal inductor with nil resistance and capacitance. In this analysis, resonance is achieved at the expense of a low quality factor (Q-factor).

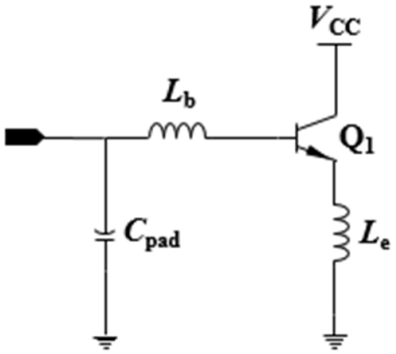

Fig. 1: Proposed IMN for the LNA with an inductively degenerated CE amplifier.

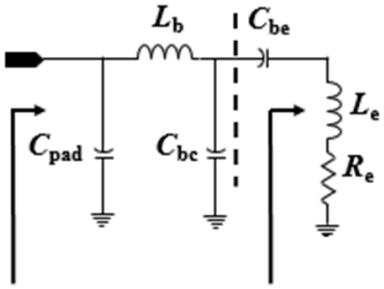

Fig. 2: Equivalent circuit model of the IMN.

The following matching conditions, (1), (2), and (3) must be satisfied [13]:

$$\omega_T \times l_e + r_e \cong R_s \tag{1}$$

$$\omega_o^2(l_b + l_e) \times (C_{be} + C_{bc}) \cong 1 \tag{2}$$

$$\omega(l_b + l_e) = \frac{1}{\omega(C_{be} + C_{bc})} \tag{3}$$

where l_e is the inductance of the base; l_b is the inductor at the base of the transistor; R_s is the input resistance of 50 ohms; r_e is the resistance of the inductor; ω_T is the unity gain frequency; ω_o is the operating frequency, C_{be} is the internal capacitance of the transistor across the base-emitter junction and C_{bc} is the internal capacitance of the transistor across the base and collector junction. It has been established in [14] that ignoring C_{bc} is not practically correct when modeling at the 60 Ghz LNA. With the above condition, the necessary values are computed for this analysis. From (2), l_e and

l_b can be determined, since the value of ω_o is known. Figure 3 is a flow chart showing the process followed in computing the resonant frequency and the input reflection loss using MATLAB. The input impedance of the IMN in Figure 1 is calculated. The resonating frequency is computed based on the initial assumption of values used at the onset of the simulation and it is updated until it resonates at the desired frequency. Thereafter, the transfer function of the system consisting of the coefficient of s at a higher degree is computed. The response of the network depends on the coefficients of s^2 and higher, as revealed in the transfer function, and this cannot be ignored. The magnitude and the phase response of any system are needed to estimate accurately and optimize the values of the parameters. If the transfer function is of a higher order in the polynomial, a second order approximation of the transfer function is computed to reduce the order of the system. Once this has been completed, a frequency response plot of the system is generated. Figure 3 is a flow chart showing the process followed in computing the resonant frequency using MATLAB.

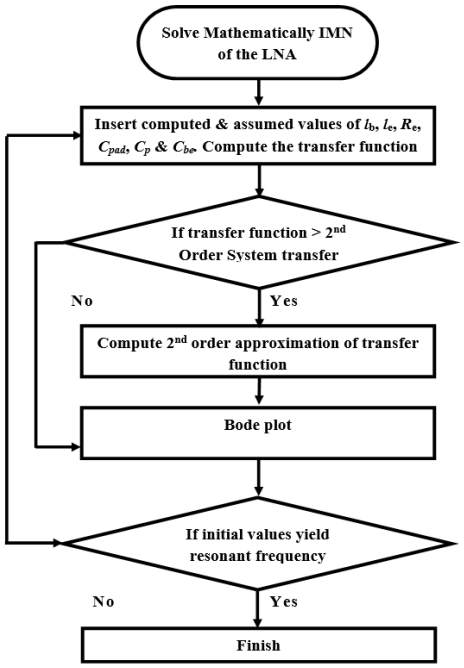

Fig. 3: Flow chart of the input matching algorithm.

The second order approximation is computed using the Taylor series, where the polynomial approximation is achieved. This response is determined solely by the s^2 and it can be mathematically described in relation to the components at the numerator of (4), where b_o is the first coefficient of the numerator with a power of zero. The expression in (4) is represented in a linear time invariant model using the transfer function model expressed in (5).

$$H(s) \approx \frac{b_o}{s^2} \tag{4}$$

$$H(s) = \frac{A(s)}{B(s)} = \frac{a_1 s^n + a_2 s^{n-1} + \cdots + a_{n+1}}{b_1 s^m + b_2 s^{m-1} + \cdots + b_{m+1}} \tag{5}$$

3 DC and AC characterization of 130 nm BiCMOS transistor

The cascode topology is reliable for balancing the parameters of the LNA such as gain, linearity, power consumption and NF. The topology used in characterizing the transistor consists of a single-stage, CE and CB transistor stacked together. In designing an LNA, the simulation of dc and radio frequency (RF) characteristics are carried out. Advantages of cascode topology include superior frequency characteristics in the absence of the usually large Miller capacitance, since it is partially cancelled out. Figure 4 shows the implementation of a cascode topology using a SiGe HBT. Identical HBTs of similar sizes, coupled with a collector voltage, V_{CC}, of 1.5 volts are used to power the circuit. The base of Q_2 is biased using the V_{CC}. A collector-base-emitter-base-collector (CBEBC) transistor layout was used, which has an area of 0.12 μm by 0.25 μm. The reduction of the width allows low power consumption and increased peak f_T. Figure 4 shows the setup for the RF and dc simulation. The idea is to match the input and output port of the schematic shown at the mm-wave frequency using the S-parameter at a unique bias point (ac and dc). The S-parameter's reading is normalized to a characteristic impedance of 50Ω. This is connected to the base of Q_1 and the collector of Q_2. In the process of extracting the S-parameters, the S-parameter control is used to sweep across multiple frequencies. The measured S-parameters include S_{11}, S_{12}, S_{21} and S_{22}. These parameters are then further used in computing the admittances, impedance and the gain as required.

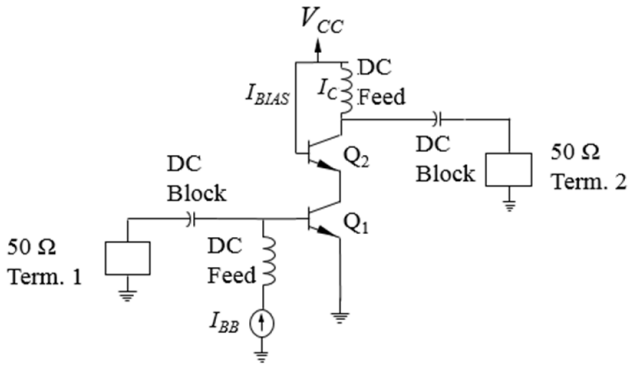

Fig. 4: Setup for RF and dc simulation for cascode topology using 2.5 μm by 0.12 μm CBEBC configuration, consisting of dc feed and dc block.

4 Design methodology of the LNA

In designing an LNA, it is imperative to maximize the gain and linearity, reduce dc power, and reduce the NF while keeping the frequency constant. In [12, 15–20], many design strategies have been utilized. The following are the design considerations and steps employed in designing a 60 GHz LNA, using a cascode topology with series peaking inductor connected across the transistors.

A. Choice of Optimum Current Density, J_{opt}

In the design of the LNA, choosing the current density at the minimum NF and the maximum f_T and f_{MAX} is necessary for determining the biasing point of the transistor. The current density is also dependent on the emitter length, since the width of the transistor is fixed. If the maximum gain is the end-goal of the design, then the circuit must be biased at the peak f_{MAX}. However, in this case, the J_{opt} values between the optimum current density at minimal noise and transition frequency are chosen. As the J_{opt} value approaches the J_{opt} value related to f_T, the shot noise associated with the LNA increases. In [21], designing an LNA using the cascode topology comprises biasing at the minimum noise current density, J_{opt}; ensuring simultaneous input impedance and optimum noise impedance match is important. This was highlighted by [11], where the biasing current, J_{opt}, was approximately equal to the peak f_T current density, similarly applied in a cascode topology.

B. Choice of Q-factor

In the design of an LNA, the choice of Q-factor is very important. Some publications have proposed a random choice, while others have employed simulations to find the appropriate Q-factor. In this design, a guiding rule that a low Q-factor serves for the ultra-wideband and mm-wave band, while a high Q-factor can be employed in the narrow band, is followed. The interdependence of the Q-factor and the gain, bandwidth, capacitance across the base and emitter, frequency at resonance, R in parallel and the inductance at the input matching is considered. The relationship between the resistance at the source, R_s, and the load resistance, R_l, can be used in the computation of the Q-factor.

C. Introduction of Inductive Degenerative Emitter

The contribution of emitter degeneration to the LNA, especially at the first stage, not only reduces the minimum NF but also stabilizes the amplifier and linearity level. Even better is the fact that the possibility of simultaneously matching the noise and impedance for an inductively generated stage can be easily realized. In order to ensure an optimally matched network, the input impedance must be equal to the complex conjugate of the optimum source impedance and source impedance. Analytically, Z_s is determined using (6) below, where Z_{in} is the input admittance, Z_{sopt} is the optimum source admittance and r_e and r_b are the resistance associated with the inductor at the emitter and base respectively. The resistive component of Z_{sopt} is used in analyzing the IMN. Computing $L_e$against the real part of the source impedance can be achieved by equating it to the ratio of the difference between $50\,\Omega$ impedance at the source and the resistance associated with the base and emitter of the transistor and the angular frequency. This is expressed in (7); where f_T is the transit frequency measured using the cascode topology.

$$Z_s = Z_{in} = Z^*_{sopt} \tag{6}$$

$$L_e = \frac{Z_0 - r_e - r_b}{2\pi f_T} \tag{7}$$

D. Computing the Capacitance across the Base and Emitter Junction and its related Transconductance.

The base-emitter capacitance, C_{be}, adversely affects the gain and noise performance of the LNA. Equation (8) shows the relationship between the C_{be}, transconduc-

tance, g_m, and angular transition frequency, ω_T:

$$C_{be} = \frac{g_m}{\omega_T} \tag{8}$$

$$L_b = \frac{\omega_T}{\omega^2 \times g_m} - L_e \tag{9}$$

$$L_b = \frac{X_{sopt}}{\omega} - L_e. \tag{10}$$

C_{be} is thereafter used in computing the transconductance of the transistor. This parameter plays a significant part in determining the overall gain of the circuit. The inductor at the base, L_b, is necessary for ensuring optimal input matching of the network. The reactive component of Z_{sopt}, expressed in (9), is used in computing the value of the inductor at the base. The inductor at the base is also dependent on the inductor at the emitter. Equation (9) can be expressed further and presented in (10).

E. Introduction of Capacitance of the Pad and Series Inductor across the CE and CB Transistor

The pad capacitance of the LNA, C_{pad}, appears as a parallel connection; at the input of the LNA, it is connected to the source impedance, Z_s. The mathematical expression for the impedance input matching is shown in (11).

$$Z_{in} = \omega_T \times L_e + j(\omega L_e + \omega L_b - \frac{\omega_T}{\omega \times g_m)} \tag{11}$$

However, this expression excludes C_{pad}, which in fact cannot be ignored. This has to be factored into the input matching of the LNA as described in [12]. Therefore, C_{pad} can be calculated by using (12). Figure 5 shows the schematic of the LNA formulated from the methodology proposed for the 60 GHz LNA. The design consists of the cascode topology with series inductor across Q_1 and Q_2. The series peaking inductor, L_{im}, connected across the CE and CB junction, is initially computed using network matching. It is thus optimized by simulating and plotting the f_T and minimum NF (f_{min}) against different values of L_{im} [15]. This approach is aimed at broad banding and increasing the bandwidth of the LNA. L_c and L_e play a significant part in determining the overall gain of the first stage. The ratio of L_c/L_e gives the power gain. It is therefore necessary for amplification that the value of L_c be larger than L_e in order to increase the gain of the first stage, as expressed in (13).

$$C_{pad} \geq \left(\frac{\omega_T}{g_m} - Z_0\frac{\omega^2}{\omega_T}\right)^{-1} \tag{12}$$

$$Gain = \frac{L_c}{L_e} \tag{13}$$

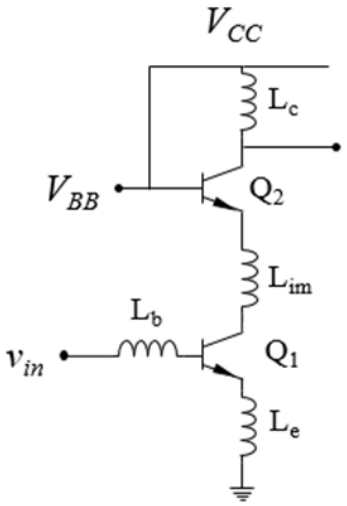

Fig. 5: LNA topology utilized in the design consisting of the cascode topology with series inductor across the transistor.

F. Design of other Stages: Multistage The design of the LNA is aimed at optimizing the f_{min} at the first stage. However, subsequent stages of the LNA are not biased at the current density aimed at the lowest NF, as stipulated in the first stage, but are biased at the higher f_T and higher J_{opt}, since other design parameters are to be optimized. These parameters include gain, bandwidth and linearity.

5 Schematics of the LNA

The schematic of a 60 GHz LNA in the V-band using a 130 nm SiGe BiCMOS HBT is depicted in Figure 6. It employs a two-stage cascode topology, which reduces the effect of the capacitance across the base and collector, C_{bc}, in the process, thus improving reverse isolation and enhancing stability. The cascode topology is made of four transistors of width $0.12\,\mu m$ and length $2.5\,\mu m$. The scaling transistor Q_1 improves the possibility of attaining optimum NF and input matching. Meshed between these stages is interstage matching consisting of a dc-block capacitor C_1, a bias and a base inductor (L_3 and L_4). Each stage consists of a series inductor (L_1 and L_5) between the CE and the CB transistor. C_{pad} represents a point of access to the LNA. Thus, it is designed as part of the IMN. Because of the very small value of C_{pad} and C_{be}, the L matching network, which consists of the L_{BIAS}, L_b effectively cancels out the capacitance of the LNA. L_e also contributes to creating a simultaneous noise and impedance matched input network. In this design, the goal at the first stage is to optimize the NF, making it as small as possible, while subsequent stages are aimed at increasing the gain of the LNA, ensuring linearity.

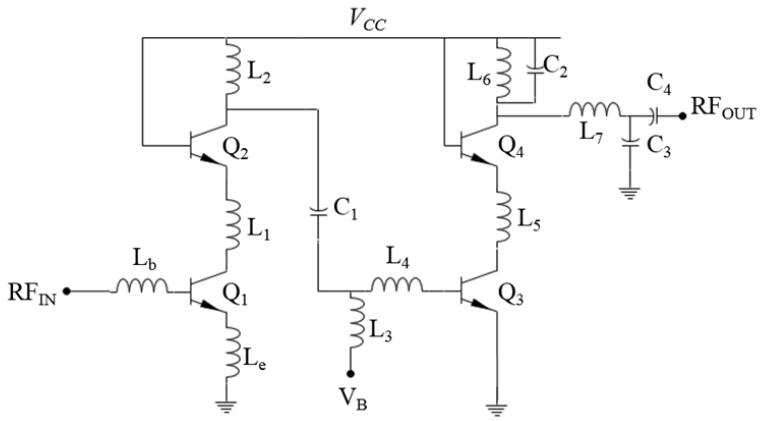

Fig. 6: Simplified circuit diagram of a two-stage cascode topology using an inductive emitter degeneration at the input matching of the first stage.

Since the width of the HBT is constant, the emitter length is varied to determine the suitable length that offers the lowest NF and the highest small-signal current gain, H_{21}, for the characterization process. In this process, the voltage across the collector-emitter, V_{CE}, and the voltage across the base and emitter, V_{BE}, of the cascode topology are kept constant. Figure 7 shows a plot of the NF and H_{21} against the emitter length. The results show that the optimal point for NF and H_{21} deviate slightly from the $2.5\,\mu m$ emitter length. The optimum noise impedance, R_{sopt}, can be estimated at about $72\,\Omega$. With R_{sopt} computed, the scaling factor, K, can be calculated. This provides a good balance for the noise and gain/linearity of the first stage. The second stage is biased to achieve a higher gain, since the emitter degeneration is no longer part of the circuit. In the IMN, the source impedance of the first stage was matched against the input matching of the first stage. This was the optimum way of calculating the values of the other components in the circuit. In order to exclude the need for any external noise matching circuit in the LNA, an inductively degenerative emitter is introduced to the HBT in the first stage.

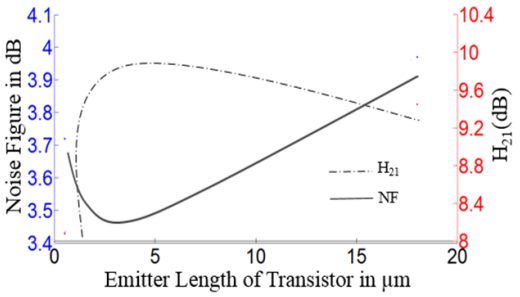

Fig. 7: Simulation result for determining the optimal length of the transistor at a constant width of $0.12\,\mu m$, V_{CE} and V_{BE} of 1.8 and 0.85 volts respectively.

The source impedance, Z_s, must be equal to the input impedance, Z_{in}, and the optimum impedance of the LNA, Z_{sopt}. This is expressed mathematically in (6), where $Z_{sopt} = R_{sopt} + jX_{sopt}$; Z_s is the source impedance of the LNA and Zin is the input impedance of the LNA.

According to (6), the difference between Z_s and Z_{sopt} is close to zero. This is only when optimum NF is achieved. The aim of the first stage is to ensure a low NF. In designing the IMN for the LNA, a CE transistor of the cascode topology is used. In this approach, a parasitic capacitance and dc-block capacitance of the input is utilized. The value of the pad capacitance ranges from 17 fF to 30 fF, as demonstrated in [12,23,24]. In this design, a parasitic capacitance of 30 fF was assumed. The values of transconductance, g_m, current gain, β, C_{be}, current at the collector, I_C, current at the base of the transistor, I_B and optimum source resistance, R_{sopt} are known. R^c_{sopt} is calculated using (14) [26].

$$R^c_{sopt} = \sqrt{\beta\left(1 + \frac{2 \times g_m \times r_b}{g_m}\right)} \tag{14}$$

$$L_e = \frac{R_s}{K \times \omega_T} \tag{15}$$

$$L_b = \frac{X^c_{sopt}}{\omega} \tag{16}$$

Once X^c_{sopt} has been computed, a scaling factor, K, is calculated by dividing X^c_{sopt} / R_s. Le can now be computed using (15), where $_T$ is the transition frequency of the transistor and X_{sopt} is dependent on C_{be}. In fact, it is the inverse of the operating frequency, ω and C_{be} of the transistor. The difference between $1/(\omega C_{be})$ and ωl_e will be used in the input matching, since $R_s = R_{sopt}$. Equation (16) expresses the relationship between the operating frequency and the inductance at the base [12], where ω and X^c_{sopt} are the operating frequency and the reactive source component of Z_{sopt}, respectively. With the resistive and reactive components of Z_{sopt} computed, impedance and noise matching has been achieved. A Smith chart can be used to extract the components of the circuit. The interstage matching network is expected to increase the bandwidth as well as gain of the LNA. A T matching network was employed, with a dc-blocking capacitor; an inductor serves as the load for the biasing voltage of 0.85 V with an inductor connected to the base of the transistor. This not only enhances the bandwidth; it reduces the NF and increases the gain. To ensure proper matching between the first and second stages, the output reflection coefficient, Γ_{OUT}, must be equal to the complex conjugate reflection coefficient at the input, Γ_{IN}. In the output stage, it is necessary to ensure that the source reflection coefficient, Γ_S, and the load reflection coefficient, Γ_L, are properly matched. Before this can be attained, the desired load reflection coefficient, Γ_L, must be selected and matched to the reflection coefficient of the output load, Γ_{OL}. This is accomplished by using the operating gain principle where power gain circles are plotted and the nearest Γ_S to the peak gain circle is selected. The governing equation is:

$$\Gamma_L = \Gamma_{OL} \tag{17}$$

6 Results and Discussion

The 60 GHz LNA was designed and simulated using a 130 nm SiGe HBT BiCMOS GlobalFoundries technology process. At a bias voltage of 0.85 V, the LNA operates at 9 mW from a supply voltage of 1.8 V. The input matching of the 60 GHz LNA was investigated with a source impedance of $50\,\Omega$. In Figure 8 and Figure 9, the ($\mid S_{11} \mid$) and ($\mid S_{22} \mid$) are lower than 14 dB and 20 dB respectively. For ($\mid S_{11} \mid$), it is below 14 dB between 57 and 64 GHz while it is lower than 12 dB in a similar frequency (57 – 64 GHz) when considering the mathematical approach used in the computation of S_{11}. This shows clearly that the mathematical approach offers some insight into the behavior and frequency response of the IMN. Figure 8 shows a plot of the ($\mid S_{11} \mid$), represented with dotted lines and a solid line for the mathematical approach and the simulation approach. Likewise, in ($\mid S_{22} \mid$), it is below 20 dB between 57 and 63 GHz. ($\mid S_{22} \mid$) within the same frequency range yielded lower than 50 dB. However, this could not be depicted in the graph. The forward gain S_{21} of the LNA depicted in Figure 10 is 26.63 dB, achieved at 60 GHz frequency. The 3 dB gain spread is across 58 – 62 dB. The gain can be attributed to the cascode stage employed in the design of the LNA. At 60 GHz, an NF of 4.3 dB was simulated, which is the lowest for the LNA, as shown in Figure 11. The stability parameter is displayed in Figure 12, as the parameter K is higher than 1 across all frequencies of interest (56 to 64 GHz). The LNA is unconditionally stable. A good reverse isolation, S_{12} at -76 dB, was simulated, as shown in Figure 13. The proposed LNA achieves the highest gain at the desired frequency range. The figure of merit (FOM), used for comparison with other LNA's is:

$$FOM = \frac{Gain \times BW[GHz]}{(NF-1) \times P_D[mW]} \tag{18}$$

where Gain is the expected power gain, NF is the expected NF, BW is the 3 dB bandwidth and P_D is the dissipated power. The proposed LNA has an average FOM of 4.48 GHz/mW. The performance of the proposed and designed 60 GHz LNA in the V-band frequency and its comparison with existing wideband LNAs are summarized in Table I.

Table 1. 130 nm SiGe BiCMOS LNA Performance Comparison with State-of-the-Art LNAs

	[1]	**[2]**	**[3]**	**[4]**	**[5]**	**[6]**	**[This work]**
Technology	65 nm CMOS	40 nm CMOS	28 nm CMOS	65 nm CMOS	90 nm CMOS	90 nm CMOS	130 nm BiCMOS
Topology	Cascode	Cascode	Cascode	CE + Cascode	CE + Cascode	Differential CE	Cascode
Gain (dB)	11.4	15	23	17.3	11.2	19.8	26.63
Power (mW)	11.2	20.4	25.3	22.8	4.04	177	9
Bandwidth (3 dB)	14	13	19	20	22.5	7	5
NF_{min}	5.6	3.6	5.8	4.9	4.8	6	4.3
FOM (*GHz/mW*)	2.59	3.68	3.60	3.89	16.41	0.11	4.48

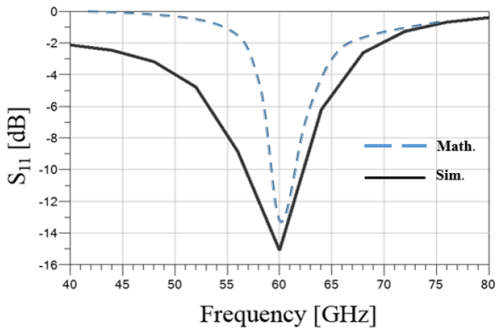

Fig. 8: Simulated S_{11} parameter of a two-stage cascode LNA.

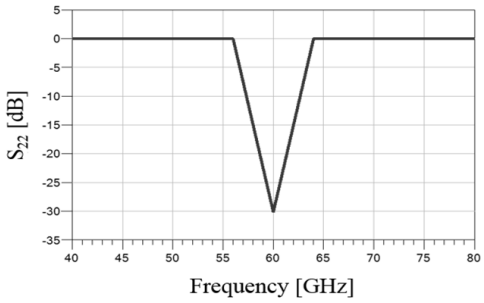

Fig. 9: Simulated S_{22} parameter of a two-stage cascode LNA

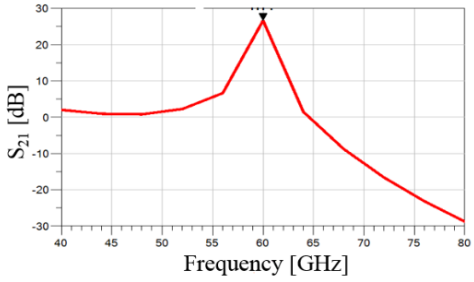

Fig. 10: Simulated S_{21} parameter of a two-stage cascode LNA.

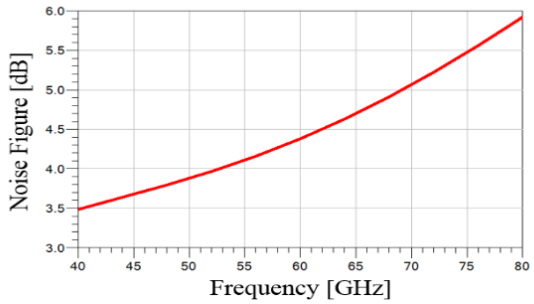

Fig. 11: Simulated NF of a two-stage cascode LNA.

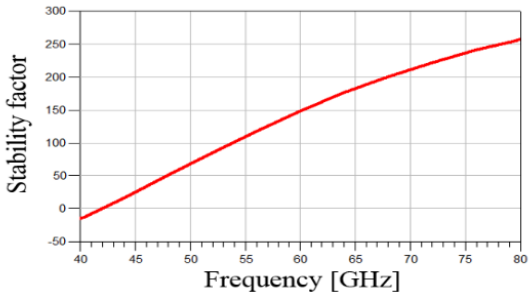

Fig. 12: Simulated K of a two-stage cascode LNA.

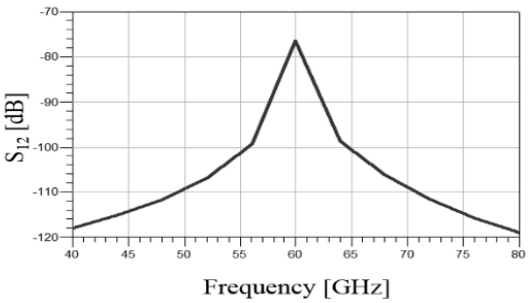

Fig. 13: Simulated S12 parameter of a two-stage cascode LNA.

7 Conclusion

In this paper, a mathematically based approach for computing the input return loss of an LNA was investigated. A flow chart, which details a step-by-step approach for designing and analyzing the input reflection coefficient was discussed. It was discovered that the input reflection coefficient plays a significant role in the performance of the IMN, while relying on the parasitic capacitance. Thereafter, a step-by-step design methodology that can be used in the design of a 60 GHz LNA was proposed. In addition, the design and simulation of a high-gain, 60 GHz LNA using lumped elements was presented. Furthermore, the design was based on a two-stage cascode SiGe HBT BiCMOS process, using ADS and demonstrating a small-signal gain of 26 dB with low power consumption of 9 mW. An NF of 4.3 dB at 60 GHz was realized. The IMN and OMN were conjugate matched by using an L-matching and T-matching matching network for maximum power output.

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