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Scaling the graphene-silicon heterojunctions: fabrication and characterization

Anca-Ionela ISTRATE , Monica VECA , Florin NASTASE , Angela BARACU , Raluca GAVRILA , Florin COMANESCU , Vasilica TUCUREANU , Adrian DINESCU , and Titus SANDU*

National Institute of Research and Development in Microtechnologies IMT Bucharest, Erou Iancu Nicolae str. 126A, 077190, Bucharest, Romania
*E-mail: titus.sandu@imt.ro

Abstract. The current work presents the fabrication and characterization of graphene-silicon heterojunctions with various contact areas. First, we transferred the graphene from copper to Si and SiO_2 substrates using Electrochemical Delamination and then we processed and characterized the transferred graphene. Second, we manufactured graphene-Si heterojunctions with several contact areas made by opening windows of various sizes in Si. Microscopy and spectroscopy analysis confirms the successful graphene transfer which is also revealed by a relative high carrier mobility of 2327 $cm^2/V{\cdot}s$ measured in a field effect transistor configuration. We test the quality of graphene-Si Schottky contacts by measuring the I-V characteristics of heterojunctions established within Si windows with linear sizes ranging from up to 70 μm to down to 6 μm. All our structures exhibit rectifying I-V curves behavior from which we were able to extract junction parameters like the ideality factor, the barrier height and the series resistance. This work provides a route to engineer graphene-based devices like Schottky diodes and field effect transistors (FETs) by relatively simple procedures.

Keywords: Graphene; Carbon materials; Electrochemical delamination; Raman; Atomic force microscopy; Diodes; Field-effect transistor; Electrical properties.

1 Introduction

Graphene (GR), a monoatomic layer of carbon atoms with ambipolar properties [1, 2], has aroused great interest in recent years because of its various applications in the fields of electrical and electronic devices, supercapacitors, solar cells, composite materials and biomaterial [4, 5]. Further, owing to its high carrier mobility (2000-4000 $cm^2/V{\cdot}$ s when supported on SiO^2/Si or hexagonal boron nitride) [3], gapless spectrum and almost frequency-independent absorption in the visible, GR is a very promising material for the development of detectors and modulators operating in the

terahertz region of the electromagnetic spectrum (wavelengths in the hundreds of micrometers) [6] and as transparent electrode [7].

Taking advantage of GR simplicity to be integrated into existing semiconducting technology corroborated with its capability to form junctions with both 2D and 3D semiconducting materials we developed small area graphene-silicon Schottky diodes. The uniqueness of these devices comes from tenability of the Schottky barrier height, characteristics which make them functional in applications like photo-detectors [8], chemical and biological sensors [9], high-speed electronic communications [10], or in circuit applications requiring high current and low voltage [11]. The challenge in the fabrication process is the ability to establish an intimate GR/Si contact by avoiding structural modifications of the semiconductor while simultaneously preserving the superior properties of graphene.

Among all known methods used to synthesize graphene (e.g. mechanical cleavage [12], chemical vapor deposition [13], graphene oxide reduction [14], or silicon sublimation from SiC crystals [15]) the most efficient and well developed method is the CVD on metallic catalyst. This method is suitable for various applications, such as microelectronics or flexible transparent electrodes [16], usually obtained by a post growth transfer of the GR from the metallic catalyst film to the substrate of interest. In order to circumvent chemical etching of metallic catalyst, a new and efficient method has been developed which consists of electrochemical exfoliation of the graphene from the metallic film [17]. To transfer GR grown on these metal substrates, etching of the metals is the efficient and straightforward way. Fe, Ru, Co, Ni, and Cu can be etched by their etchants easily. But, for the chemically insert or noble metal substrates, such as Ir, Pt, and Au, the traditional wetting transfer methods are not available, because these metals are difficult to be etched away completely or the cost is too high. The Electrochemical Delamination method, which will be discussed later seems to be an efficient way to transfer GR grown on these metal substrates [18].

However, all the wet transfer methods will usually introduce impurities (chemical contamination) which will give GR with electronic mobility of 500 to 104 cm^2 V^{-1} s^{-1} and high concentrations of p-type dopants ($\sim 10^{12}$ cm^{-2}). For this particular reason before using the graphene in the proposed device we have evaluated its conducting properties in the FET devices.

Graphene/silicon (GR/Si) configurations for optoelectronics have thus drawn considerable attention. Because of the work function difference between GR and silicon, their contact results in charge transfer, yielding a built-in electric field [7]. Here we fabricated various GR/Si diodes by transferring graphene over pre-patterned square silicon windows with linear size between 70 and 6 μm.

Intrinsic electrical properties like carrier mobility and transconductance for GR were estimated in a standard back-gated FET geometry, while the electrical properties of GR/Si hetero-structures like ideality factor (η), barrier height (Φ_B), and series resistance (R_S) for GR/Si diodes were calculated from the I-V characteristics. Schottky contacts were successfully obtained down to windows size of 6 μm $\times$ 6 μm.

In the following we will describe the graphene transfer from copper to n-type Si substrate and to SiO_2 using Electrochemical Delamination, for manufactured several GR-Si junctions with square geometry and side lengths of: 6 μm, 20 μm, 40 μm and 70 μm placed on the same chip and GR FET with channel length of 60 μm. The quality of the transferred graphene was assessed from Raman fingerprints of GR allowing the identification of defects density. The characterizations by optical, atomic force and scanning electron microscopy revealed also the transfer efficiency of GR flakes. Finally from I-V electrical measurements of GR-Si and GR-SiO_2/Si heterojunctions we calcu-

lated carrier mobility and all Schottky diode parameters. The conclusions are outlined in the last section.

2 Experimental Details

2.1 Transfer process of graphene

The monolayer GR on copper foil (GR/Cu) was provided by *Graphene Supermarket*. The GR on copper were transferred to Si and SiO_2/Si by *Electrochemical Delamination* method using a home-made system described elsewhere [19]. Briefly as received GR/Cu was firstly coated with 300 nm PMMA film, backed at 150°C for 2 minutes and thereafter used as the cathode in the electrochemical cell (graphite | 0.05 mM $K^2S^2O^8$| GR/Cu). An electrical potential of 40 V was applied to the cell and an average current of 1 mA was recorded. We noticed after 10 minutes the entire film of PMMA/GR was floating on the surface of electrolyte solution and collected on the device of interest (FET or diode).

2.2 Fabrication of graphene-Si junctions and graphene FETs

We noticed that 300 nm SiO_2 thickness does not allow direct contact between GR and silicon substrate for small area windows. Thus, in order to increase the contact area of GR/Si junctions presented in our previous report [19] we changed the SiO_2 thickness from 300 nm to 100 nm. The lightly doped n-type <100> Si wafers with 1-5 Ω·cm resistivity have been used as substrates in order to manufacture the GR/Si junction. After a standard cleaning process, a thin film of 100 nm SiO_2 has been grown, a reduced thickness was selected in order to promote conformal contact between the graphene and the semiconductor. The metal contact consisting of Cr/Au, with a thickness of 10/100 nm has been deposited by DC Sputtering. After SiO_2 back side etching, the metallic film has been patterned (Figure 1) right). Then, a second mask has been used to etch the SiO_2 on the front side of the wafer, in order to open the Si contact windows in the SiO_2 layer. The next step has been the back contact fabrication by DC Sputtering of Cr/Au with 20/40 nm thickness. Finally, GR has been transferred by Electrochemical Delamination in order to obtain GR-Si junction with square windows having linear sizes of 70 μm, 40 μm, 20 μm and 6 μm placed on the same chip.

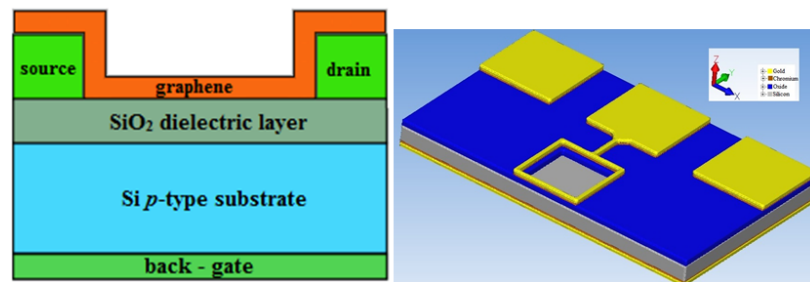

Fig. 1: Schematic depicting a device configuration before graphene transfer: (left) Schematic back-gated graphene field-effect transistor and (right) template geometry for graphene-Si heterojunction; the active areas are square windows with predeposited Au line contacts around.

Owing to the van der Waals forces graphene recovered after electrochemical delamination, have firmly adhered on the metal contact as well as on the silicon semiconductor (showing a low resistance ohmic contacts with the gold).

The GR-FET was obtained by transferring graphene on the channel area of the FET structure purchased from Ossila Figure 1 (left). The standard back-gated FET structure, use thermally grown SiO_2 (300 nm) on highly p-doped (Boron) silicon as the starting substrate and thermally-evaporated gold electrodes.

The Schottky diodes were fabricated by placing graphene on top of Si/SiO_2/Cr/Au structure schematically presented in Figure 1 (right). The native oxide within the window area was removed by BOE (buffered oxide etching solution) with a subsequent drying to remove any water from the surface.

2.3 Characterization

The structure analysis of GR on copper foil was carried out using Fourier Transform Infrared spectroscopy (FTIR) using a Bruker Optics Vertex 80V Spectrometer, equipped with a transmission accessory. IR spectra were recorded after 64 scans with a 4 cm^{-1} resolution, in a spectral range of 4000-400 cm^{-1}. Transferred GR was investigated by means of micro-Raman Spectroscopy, Horiba Labram Hr 800 equipment with 633 nm He-Ne laser. Atomic Force Microscope (NTEGRA Aura – NT-MDT model) and Scanning Electron Microscopy (Nova NanoSEM 630) were used to study the surface topography and morphology of transferred GR. The electrical characteristics of GR-Si hetero-junctions were measured with 4200-SCS/C/Keithley system.

3 Results and Discussion

3.1 FTIR spectrometry

The FT-IR peaks of GR are shown in Figure 2 at 2980 cm^{-1}, 2903 cm^{-1}, 1653 cm^{-1}, 1449 cm^{-1}, 1398 cm^{-1}, 889 cm^{-1}, 711 cm^{-1} and 658 cm^{-1}.

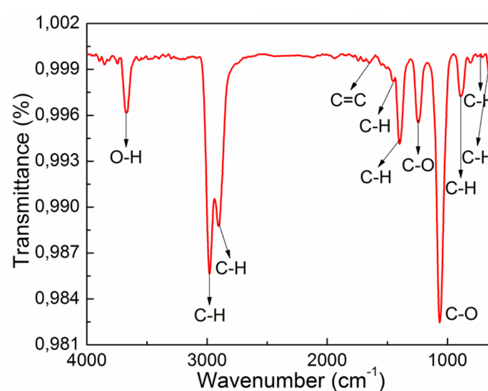

Fig. 2: FT-IR spectrum of as-grown graphene on copper foil.

The presence of peaks observed at 2980, 2903 si 1449, 1398, 711, 658 cm^{-1} can be atributted to vibrations mode and respectively, C-H bond formation from metilen group. The presence of peaks observed at 3650 cm^{-1} (O-H stretching vibrations) and at

1242 cm^{-1}, 1064 cm^{-1} (stretching vibrations from C-O) [20,21] is a strong indication of the oxidation of GR sheets on copper by oxygen-containing groups: hydroxyl group and epoxy group. The peak at 3650 cm^{-1} was from the O-H groups due to H_2O or O_2 remaining in GR sheet. These vibrations indicate that O-H and C-O groups were anchored to the GR sheets and could lead to undesirable functionalized GR.

3.2 Raman Spectroscopy

Raman spectroscopy is a useful technique to analyze the transferred GR onto Si and SiO_2/Si. The Raman Spectra performed on GR sheet after being transferred on to Si substrate is shown in Figure 3. In inset it is shown the optical micrograph of GR after the transfer on Si windows with a side length of 40 μm. GR flakes are visible on SiO_2 because of a better optical contrast on SiO_2 with respect to Si.

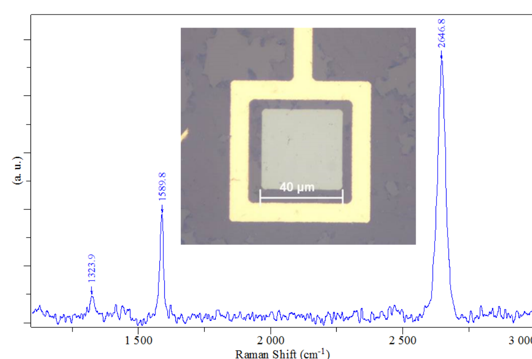

Fig. 3: Raman Spectra of GR transferred on Si window. In inset, optical micrograph of a GR after has been transferred on Si junction fabricated with square geometry with side length of 40 μm.

Another evidence of the transferred graphene integrity on the silicon area is the recorded Raman spectrum presented in Figure 3. It reveals the presence of the characteristic bands of GR (D $\sim$1323.9 cm^{-1}, G $\sim$1589.8 cm^{-1}, 2D $\sim$2646.8 cm^{-1}). In addition the intensity ratio between the second order and first vibrational order band combine with the narrow 2D band (FWHM – 2D = 34.13 cm^{-1}) are clear indications of the monolayer graphene and reduced disorder/defects introduced by the transfer process. The Raman bands and the extracted parameters (I_{2D}/I_G and FWHM-2D) are confirming the existence of monolayer GR on silicon areas. The GR quality indicator ($I_{2D}/I_G \sim 2.45$) corresponding values and FWHM of 2D band which is 34.13 cm^{-1} are confirming the presence of monolayer GR on silicon areas on the sample. The $I_D/I_G \sim 0.24$ indicate a lower density of defects. The Raman analysis on copper foil (not shown here), was free of GR after transfer, this means the transfer method allows reuse of the copper foil, in multiple growth and delamination cycles.

3.3 Atomic force microscopy and Scanning electron microscopy

Surface topography images of GR film transferred to Si, (see Figure 4 top side) by Electrochemical Delamination are confirming the successful GR transfer.

The morphology of GR transferred on the silicon window is fairly smooth, making it possible to identify the GR islands, mostly monolayer, Figure 4 (top side). Few sub

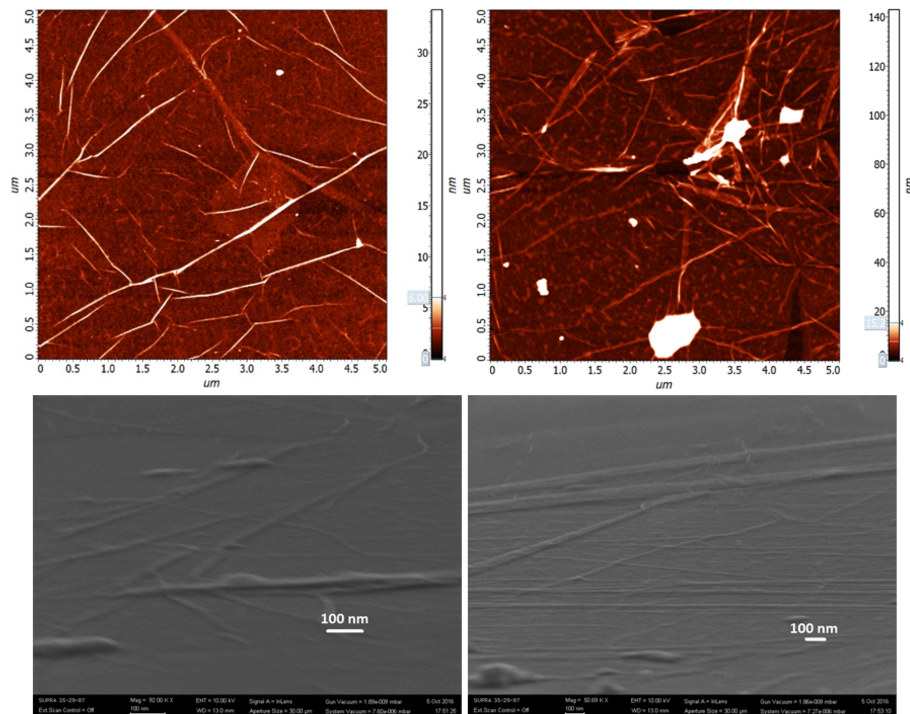

Fig. 4: (Top side) Atomic force microscopy (AFM) surface images of the GR on Si and (bottom side) SEM images of the surface of GR sheet after transfer from Cu foil.

micrometer features can be also observed on the GR, features which can be attributed to contaminations (polymer residues) left by the incomplete removal of the support polymer (PMMA employed for the transfer process). The SEM image shown in Figure 4 (bottom side) illustrates specific features of GR, bumps and ripples created during the transfer process. Therefore AFM and SEM analysis concluded that GR film has been transferred onto Si.

3.4 Electrical characterization of GR-FET

Electrical measurements have been also performed on GR field effect devices with a channel of 60 μm after GR transfer Electrical properties of graphene refer especially to doping (the level and type) and to carrier mobility. For device applications graphene are doped p-type or n-type by chemical or electrostatic procedures. Similar to wide bandgap semiconductors [22], p-doping occurs naturally for graphene but n-doping is more difficult to achieve [23].

Figure 5 shows the output characteristics of a GR FET with a width of W = 1 μm at zero gate voltage and at Vg=10 – 30 V, respectively Vg= -10 – -30 V. The drain current increases linearly with increasing drain bias. The I-V plots in Figure 5 are asymmetric with respect to the polarity of Vg, indicating that the minimum electrical resistance between source and drain is obtained for positive gate voltage, hence the graphene sheet is *p*-doped [24].

We calculated the mobility of GR with a FET configuration with 60 μm channel

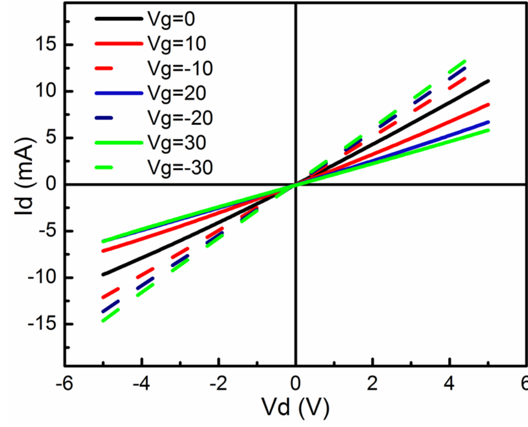

Fig. 5: The Id-Vds curve of graphene FET with 60 μm channel length

length by the direct transconductance method based on the transfer characteristic from field-effect measurements of GR according to the equation [25]:

$$\mu = \frac{g_m}{V_{ds} \cdot C_{ox}} \cdot \frac{L}{W}, \quad (1)$$

where μ is the field-effect mobility, g_m is transconductance, V_{ds} is drain-source voltage, C_{ox} is the oxide capacitance, L= channel length, W= width. In Eq. (1)

$$g_m = \frac{dI_D}{dV_g}\Big|_{V_{ds}=const}, \quad (2)$$

where I_D is the drain current, V_g is the gate voltage and

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}. \quad (3)$$

For oxide thickness t_{ox} = 300 nm we obtain an oxide capacitance of

$$C_{ox} = 11.5 \times 10^{-9} Fcm^{-2} \quad (4)$$

where ε_{ox} is the oxide permittivity, t_{ox} is the oxide thickness [26].

The GR FET with 60 μm channel length exhibits a mobility of 2327 $cm^2/V \cdot s$ and a transconductance of 22.3×10^{-6} S exceeding other reported mobility values, for example: the carrier mobility of silicon MOSFETs can be as low as 100 cm^2/V· s [27], while the carrier mobility of dual-gated bilayer GR on SiO_2 is found to be between 1.500 and 2.000 cm^2/V·s [28] or the carrier mobility of other GR FETs, 1614 cm^2/V·s to 1994 cm^2/V·s [29].

3.5 Electrical analysis of Schottky contacts

The I-V characteristics of the fabricated devices are measured for various windows with side lengths from 6 to 70 μm and presented in 6.

Since the graphene film is p-doped a Schottky junction can be formed when the graphene is in contact with an n-type silicon substrate, which can be seen in 6, where the I-V characteristic shows a room temperature rectifying behavior. Even though the

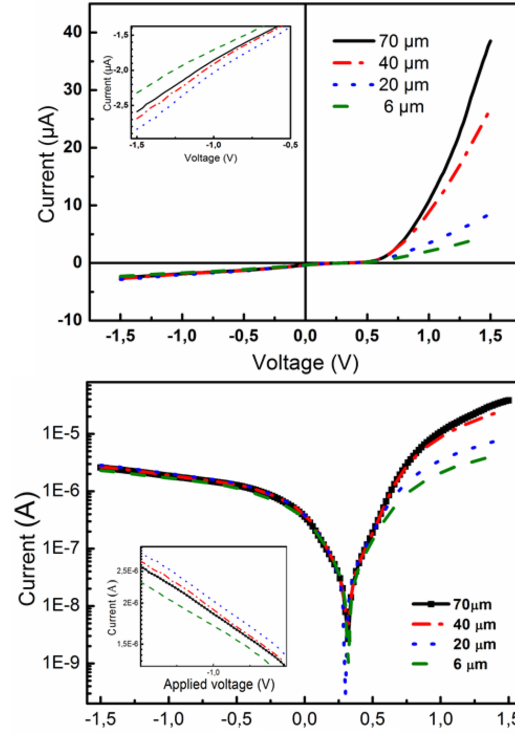

Fig. 6: I-V characteristics of GR-Si diode on 6-70 m side length (top side linear plot and down a semi-log plot). The zoom of the negative voltage are shown in the insets.

full characterization would imply temperature dependent I-V measurements we estimated Schottky contact parameters by using the I-V relationship of a Schottky barrier diode.

The *I-V* characteristic for a Schottky diode is given by the following equation [30]:

$$I = I_0[exp(qV/\eta kT) - 1], \tag{5}$$

where I_0 the saturation current is given by:

$$I_0 = AA^* T^2 exp(-q\Phi_b/kT) \tag{6}$$

In equations (5) and (6) k is the Boltzmann constant, T is the absolute temperature, q is the elementary electric charge, V the applied voltage, η the ideality factor of a Schottky diode, A the device area, Φ_b barrier height, and A^* is the effective Richardson constant, which is 112 A/cm^2/K^2 for n-type Si [31], [32]. The contact area of the device was taken to be the area of the silicon window where the contact between the graphene and silicon takes place. Considering an ohmic contact between graphene and gold electrode, and the fact that our device has a series resistance (R_s), equation (5) takes the form:

$$I = I_0[exp(q(V - IR_s)/\eta kT) - 1] \tag{7}$$

where the IR_s is the voltage drop across the series resistance of device. The values of series resistance were calculated using Cheung and Cheung's method [33] in which

the last term -1 is neglected with respect to the exponential function for large V in equation (7). The values of the series resistance and the ideality factor are determined by the following equation:

$$dV/D(lnI) = \eta kT/q + IR_s \tag{8}$$

as the slope and the intercept of the above equations. The barrier height (Φ_b) can be estimated by building the function $H(I)$ according to the equation:

$$H(I) = V - \big(\eta kT\big) ln\bigg(\frac{I}{AA^{*}T^{2}}\bigg). \tag{9}$$

The barrier height is the deduced from the following equation:

$$H(I) = R_s I + \eta\Phi_b \tag{10}$$

which gives the series resistance as byproduct. Our calculations show that the values of series resistance calculated with equation (8) match the values calculated with equation (10). The value of junction parameters: ideality factor, barrier height and series resistance computed are presented in Table 1.

The ideality factor for GR-Si diodes are in the range from 3.4–3.8. An ideality factor, η=1 corresponds to an ideal Schottky diode with purely thermionic charge transport across the barrier. The η values for GR Schottky junctions reported to date are far from ideal and are in the range $\sim$1.3-30 [34].

Table 1: The junction parameters: ideality factor, barrier height and series resistance

Side lengths of GR-Si diodes (μm)	The ideality factor, μ	The barrier height, b [eV]	The series resistance, Rs [k]
70	3.8	0.68	12.5* (13.60)**
40	3.5	0.66	22 (22.51)
20	3.6	0.62	80 (82.5)
6	3.4	0.57	164 (160)

* The values presented here are calculated with eq. (8).

** The values presented in the parenthesis are calculated with eq. (10).

The barrier height decreases, from 0.68 to 0.57 eV corresponding to diodes made within the windows with linear sizes spanning from 70 to 6 μm. Other papers reported barrier heights around 0.7 eV [35]. Since the barrier height is the difference between the graphene work function and the electron affinity of silicon (4.05 eV), our estimated barrier height lays in the range of the reported values, taking into account the fact that the graphene work function can vary from 4.4 to 4.8 eV [35]. We attribute this degradation to the scattering introduced by the surface impurities or possibly due to bumps and ripples created during the transfer process, more pronounced when side length of diode is 20 and 6 μm.

A high carrier mobility device requires special conditions for graphene, like working in an atmosphere free of contaminants on suspended graphene [37]. Defects on GR surface, as demonstrated by the FTIR analysis, would result in junctions parameters alterations. Furthermore, residual polymer (here, poly(methyl methacrylate), PMMA) left on GR from transfer or device fabrication processes affects the electrical performance of GR field-effect transistors fabricated on SiO_2/Si according to Ji Won Suk et al. [38]. This could be another reason for barrier height value decreasing from 0.68 to

0.57 eV corresponding to side lengths of GR-Si diodes from 70 m to 6 m. An additional reason could be the effective contact area for the small window side lengths (20 m and 6 m). For these small areas graphene would not follow conformal geometry of the window. It is known from the literature that the graphene makes successful membranes over 2 m wide trenches [39] Therefore we may infer that for the windows below 6 6 mm the graphene cannot make a good and reliable contact with the substrate.

The series resistance (R_s) for obtained samples presented in *Table 1*, degrades from 12.5 to 164 kΩ as side length of GR-Si diode decreased from 70 to 6 —μm. The wide non-linear *I-V* characteristic of GR-Si junction could be due to high series resistance of the device (20 μm, 6 μm). If the series resistance is low, the non-linear region will be narrow [40] as in our case GR-Si junction for side length (70 μm, 40 μm). As the effective Schottky contact area decreases Rs should increase and is given mainly by the substrates which is 500 μm thick.

4 Conclusions

In summary, this experimental work confirms the successful graphene transfer from Cu foil to the target, either Si or SiO_2 substrates, by Electrochemical Delamination using a home-made system of contacting electrodes.

The GR transferred to Si has been used to manufacture graphene-Si diodes with square geometry of different side lengths: 6 μm, 20 μm, 40 μm and 70 μm. The graphene transferred to SiO_2 has been used to evaluate the carrier mobility in a field effect transistor configuration with a channel length of 60 μm.

The FTIR spectrometry indicates the oxidation of graphene sheets on copper by oxygen-containing groups like hydroxyl and epoxy groups. The infrared spectra indicate that O-H and C-O groups were anchored to the graphene sheets and could lead to undesirable functionalized GR affecting the electrical properties of graphene based devices.

The Raman spectroscopy has confirmed the presence of single layer graphene flakes on silicon and on SiO_2 areas. After transfer the copper foil is free of graphene, hence the transfer method allows the reuse of the copper foil in multiple growth and delamination cycles.

The quality of graphene has been evaluated by microscopy techniques, spectroscopic analysis, and electrical measurements. The quality of the Schottky contacts were studied by analyzing the effect of the Si window sizes on the ideality factor, the barrier height, series resistance.

I-V characteristics have confirmed the continuity of graphene on the target substrate. The resulting *I-V* characteristics exhibit rectifying diode behavior similar to a Schottky diode. The graphene field effect transistor with 60 μm channel length yields a mobility of 2327 $cm^2/V \cdot s$ and a transconductance of 22.3×10^{-6}S, both being comparable with the literature.

Finally, we make some remarks regarding the impact of our study and future work. The present work has shown that relatively simple procedures can be followed in order to fabricate graphene-based devices like Schottky diodes and field effect transistors. Moreover, graphene-based Schottky diodes can be used as solar cells [35] or as photodiodes with higher efficiency of photon conversion by microstructuring the silicon substrate like it has been done in a quite recent paper [41]. Future work would be conducted to assess the optical properties, in general, and photon conversion efficiency, in

particular, of the Schottky diodes fabricated and presented above.

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References

[1] E. Pallecchi, F. Lafont, V. Cavaliere, F. Schopfer, D. Mailly, W. Poirier, A. Ouerghi, High Electron Mobility in Epitaxial Graphene on 4H-SiC(0001) via post-growth annealing under hydrogen, Scientific Reports 4, pp. 1-7, 2014.

[2] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, M. I. Katsnelson, I. V. Grigorieva, S. V. Dubonos, A. A. Firsov, Two-dimensional gas of massless Dirac fermions in graphene, Nature 438, pp. 197200, 2005.

[3] Graphene Science Handbook: Nanostructure and Atomic Arrangement, Edited by Mahmood Aliofkhazraei, Nasar Ali, William I. Milne, Cengiz S. Ozkan, Stanislaw Mitura, Juana L. Gervasoni, CRC Press, 2016, ISBN 9781466591370.

[4] Camila L.C. Rodriguez, Felipe Kessler, Nileshkumar Dubey, Vinicius Rosa, Guilhermino J.M. Fechine, CVD graphene transfer procedure to the surface of stainless steel for stem cell proliferation , Surface & Coatings Technology 311, pp. 1018, 2017.

[5] Jun-Hua Meng, Xin Liu, Xing-Wang Zhang, Yue Zhang, Hao-Lin Wang, Zhi-Gang Yin, Yong-Zhe Zhang, Heng Liu, Jing-Bi You, Hui Yan, Interface engineering for highly efficient graphene-on-silicon Schottky junction solar cells by introducing a hexagonal boron nitride interlayer, Nano Energy 28, pp. 4450, 2016.

[6] L. Vicarelli, M. S. Vitiello, D. Coquillat, A. Lombardo, A. C. Ferrari,W. Knap, M. Polini,V. Pellegrini and A. Tredicucci, Graphene field-effect transistors as room-temperature terahertz detectors, Nature Materials, 11, pp. 865-871, 2012.

[7] Xiaojuan Wang, Dong Li, Qichong Zhang, Liping Zou, Fengli Wang, Jun Zhou, Zengxing Zhang, Study on the graphene/silicon Schottky diodes by transferring graphene transparent electrodes on silicon, Thin Solid Films 592, pp. 281286, 2015.

[8] M. Amirmazlaghani, F. Raissi, O. Habibpour, J. Vukusic, and J. Stake, Graphene-Si Schottky IR Detector, IEEE J. Q. Electr., 49, pp.489-494, 2013

[9] Y. Liu, X. Dong, and P. Chen, Biological and chemical sensors based on graphene materials, Chem. Soc. Rev., 41, pp. 2283-2307, 2012.

[10] T. Mueller, F. Xia, and P. Avouris, Graphene photodetectors for high-speed optical communications, Nat. Photonics, 4, pp. 297-301, 2010.

[11] H Zhu, A. Liu, F. Shan, W. Yang, C. Barrow, and J. Liu, , Direct transfer of graphene and application in low-voltage hybrid transistors, RSC Adv., 7, pp. 21722179, 2017.

[12] Rostislav V. Lapshin, STM observation of a box-shaped graphene nanostructure appeared after mechanical cleavage of pyrolytic graphite, Applied Surface Science 360, pp. 451460, 2016.

[13] Nobuo Tajima, Tomoaki Kaneko, Jun Nara, Takahisa Ohno, A first principles study on the CVD graphene growth on copper surfaces: A carbon atom incorporation to graphene edges, Surface Science 653, pp. 123129, 2016.

[14] E.C. Vermisoglou, T. Giannakopoulou, G. Romanos, N. Boukos, V. Psycharis, C. Lei, C. Lekakou, D. Petridis, C. Trapalis, Applied Surface Science 392, pp. 244255, 2017.

[15] Seong-Yong Cho, Hyun-Mi Kim, Min-Hyun Lee, Do-Joong Lee, Ki-Bum Kim, Direct formation of graphene layers on top of SiC during the carburization of Si substrate, Current Applied Physics 12, pp. 1088-1091, 2012.

[16] X.M. Ge, Y.H. Zhang, Z.Y. Chen, H.R. Zhang, L. He, Y.P. Sui, R.X. Deng, G.H. Yu, Effects of Cu substrate surface fluctuations on graphene during transfer, Materials Letters 185, pp. 156160, 2016.

[17] Yu Wang, Yi Zheng, Xiangfan Xu, Emilie Dubuisson, Qiaoliang Bao, Jiong Lu, Kian Ping Loh, Electrochemical Delamination of CVD-Grown Graphene Film: Toward the Recyclable Use of Copper Catalyst, ACS Nano 5, pp 99279933, 2011.

[18] Yi Chen, Xiao-Lei Gong, Jing-Gang Gai, Progress and Challenges in Transfer of Large-Area Graphene Films, Adv. Sci. 3, pp. 1-15, 2016.

[19] A.-I. Istrate, M. Veca, F. Nastase, A. Baracu, R. Gavrila, F. Comanescu, Toward fabrication of graphene based devices: graphene transfer, processing and characterization, CAS 2016 Proceedings, pp. 159-161, ISBN: 978-1-5090-1207-7, CFP16CAS-ART.

[20] Yuxi Xu, Hua Bai, Gewu Lu, Chun Li and Gaoquan Shi, Flexible Graphene Films via the Filtration of Water-Soluble Noncovalent Functionalized Graphene Sheets, J. Am. Chem. Soc. 130, pp 58565857, 2008.

[21] Nikolina A. Travlou, Kavindra Singh, Enrique Rodrguez-Castelln and Teresa J. Bandosz, Cu-BTC MOF / Graphene-based hybrid materials as low concentration ammonia sensors, J. Mater. Chem. A 3, pp. 11417-11429, 2015.

[22] R. Plugaru, T. Sandu, N. Plugaru, First principles study and variable range hopping conductivity in disorderedAl/Ti/Mn-doped ZnO, Results in Physics 2, pp. 190197, 2012.

[23] D. M. N. M. Dissanayake, A. Ashraf, D. Dwyer, K. Kisslinger, L. Zhang, Y. Pang, H. Efstathiadis, and M. D. Eisaman, Spontaneous and strong multilayer graphene n-doping on soda-lime glass and its application in graphene-semiconductor junctions, Sci. Rep. 6, pp. 21070-7, 2016.

[24] N. Basov, M.M. Fogler, A. Lanzara, F. Wang, and Y. Zhang, Colloquium: graphene spectroscopy, Rev. Mod. Phys. 86, pp.959, 2014.

[25] Hua Zhong, Zhiyong Zhang, Haitao Xu, Chenguang Qiu, and Lian-Mao Peng, Comparison of mobility extraction methods based on field-effect measurements for graphene; AIP Advances 5, pp. 057136-1 - 057136-8, 2015.

[26] Sam Vaziri, Fabrication and Characterization of Graphene Field Effect Transistors; Master Thesis, 2011.

[27] Frank Schwierz, Graphene transistors, Nature Nanotechnology, 5, pp. 487-496, 2010.

[28] Thiti Taychatanapat, Pablo Jarillo-Herrero, Electronic Transport in Dual-Gated Bilayer Graphene at Large Displacement Fields, Physical Review Letters 105, pp. 166601-1 - 166601-4, 2010.

[29] Zhiyong Zhang,Huilong Xu, Hua Zhong, Lian-Mao Peng, Direct extraction of carrier mobility in graphene field-effect transistor using current-voltage and capacitance-voltage measurements, Applied Physics Letters 101, pp. 213103-1 - 213103-4, 2012.

[30] T. Klcoglu, Effect of an organic compound (Methyl Red) interfacial layer on the calculation of characteristic parameters of an Al/Methyl Red/p-Si sandwich Schottky barrier diode, Thin Solid Films 516, pp. 967-970, 2008.

[31] E. Marl, A. Kaya, H.G. etinkaya, S. Koyiit, . Altndal, On the temperature dependent forward bias currentvoltage (IV) characteristics in Au/2

[32] B. Bati, The Electrical Properties of Al/Methylene-Blue/n-Si/Au Schottky Diodes, Journal of Modern Physics 7, pp. 1-6, 2016.

[33] S.K. Cheung, N.W. Cheung, Extraction of Schottky diode parameters from forward current-voltage characteristics, Appl. Phys. Lett. 49, pp. 85-87, 1986.

[34] Dhiraj Sinha, Ji Ung Lee, Ideal Graphene/Silicon Schottky Junction Diodes, Nano Lett. 14, pp. 46604664, 2014.

[35] D. Xu, X. Yu, L. Yang, D. Yang, Interface engineering of Graphene-Silicon heterojunction solar cells, Superlatt. Microstr. 99, pp. 3-12, 2016.

[36] S. Parui, R. Ruiter, P. J. Zomer, M. Wojtaszek, B. J. van Wees, and T. Banerjee, Temperature dependent transport characteristics of graphene/n-Si diodes, J. Appl. Phys. 116, pp. 244505-6, 2014.

[37] K. I. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, J. Honec, P. Kima, and H. L. Stormer, Ultrahigh electron mobility in suspended graphene, Solid State Comm., 146, pp. 351355, 2008.

[38] Ji Won Suk, Wi Hyoung Lee, Jongho Lee, Harry Chou, Richard D. Piner, Yufeng Hao, Deji Akinwande, and Rodney S. Ruoff, Enhancement of the Electrical Properties of Graphene Grown by Chemical Vapor Deposition via Controlling the Effects of Polymer Residue, Nano Lett. 13, pp. 14621467, 2013.

[39] J. S. Bunch, A. M. van der Zande, S. S. Verbridge, I. W. Frank, D. M. Tanenbaum, J. M. Parpia, H. G. Craighead, P. L. McEuen, Electromechanical Resonators from Graphene Sheets, Science, 315, pp. 490-493, 2007.

[40] R.K. Gupta, K. Ghosh, P.K. Kahol, Temperature dependence of currentvoltage characteristics of goldstrontium titanate thin film Schottky diode, Physica E 42, pp. 1509-1512, 2010.

[41] Y. Gao, et al., Photon-trapping microstructures enable high-speed high-efficiency silicon photodiodes, Nat. Photonics, 2017 DOI: 10.1038/NPHOTON.2017.37.